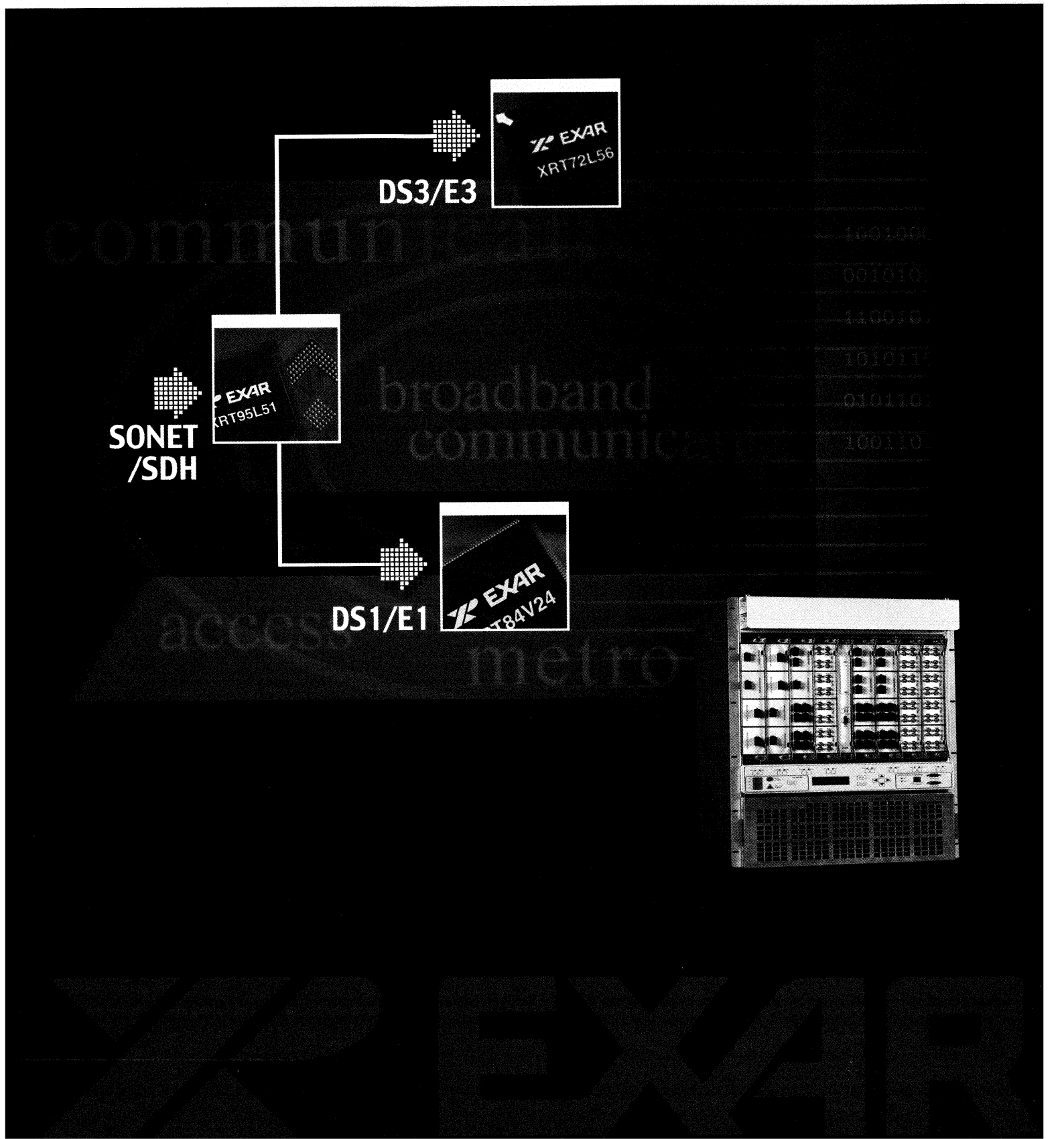
EXAR

2001-2002 COMMUNICATIONS SHORT FORM CATALOG



EXAR

2001—2002

Exar Communications Products

Short Form Catalog

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Patent Information

Exar Corporation's products are protected under one or more of the following U.S. Patents:

4,617,535, 4,771,188, 4,789,838, 4,851,893, 4,866,397, 4,949,150, 5,016,080, 5,011,784, 5,023,194, 5,068,702, 5,097,309, 5,148,395, 5,152,842, 5,190,884, 5,229,664, 5,247,581, 5,248,624, 5,315,264, 5,319,704, 5,325,045, 5,325,069, 5,357,379, 5,371,419, 5,387,877, 5,389,829, 5,440,254, 5,444,242, 5,446,412, 5,452,711, 5,502,746, 5,506,532, 5,512,816, 5,552,732, 5,557,481, 5,570,049, 5,572,212, 5,587,684, 5,592,167, 5,604,452, 5,625,281, 5,648,972, 5,650,747, 5,689,259, 5,694,031, 5,698,970, 5,703,524, 5,708,536, 5,007,081, 5,790,393, 5,796,361, 306,444, 3,883,889, 4,042,953, 4,152,823, 4,247,951, 4,265,935, 4,318,118, 4,566,914, 4,975,386, 5,283,579, 5,294,927, 5,298,814, 5,649,122, 5,801,587, 5,801,593, 5,805,005, 5,818,271, 5,528,330, 5,844,431, 5,852,360, 5,864,257, 5,870,002, 5,880,690, 5,880,632, 5,910,739, 5,914,627, 5,914,632, 5,923,203, 5,923,206, 5,929,799, 5,933,056, 5,949,787, 5,959494, 6,031,389, 6,121,805, 6,127,956, 6,121,837

There are other U.S. and foreign patents pending.

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Company Background

Exar designs, develops and markets high-performance, high-bandwidth analog and mixed-signal silicon solutions for the worldwide communications infrastructure. The Company uses its high-speed, analog and mixed-signal design expertise, system-level knowledge and standard CMOS process technologies to offer ICs for the communications markets that address Wide Area Network (WAN) transmission standards, such as T/E carrier, ATM and SONET/SDH. Additionally, Exar provides solutions for the serial communications market as well as the video and imaging markets. Exar's major customers include Alcatel, Cisco, Hewlett-Packard, Lucent, Nokia and Tellabs. The Company, based in Fremont, CA, had fiscal 2001 revenues of $113 million and employs approximately 288 people worldwide.

Communications Market and Exar's Solution

The majority of installed communications systems were designed to transmit only voice communications, and, therefore, they are inadequate for the high-bandwidth transmission of both voice and data. As a result, new equipment is being deployed to augment existing transmission media and increase overall system bandwidth. Access to the public network is typically based on asynchronous technologies, such as T/E carrier over copper wire. The demand for greater bandwidth is driving a migration from lower-speed T1/E1 (1.5Mbps/2.0Mbps) to higher-speed T3/E3 (45Mbps/34Mbps) transmission rates. The backbone of the public network is built on an optical fiber transmission medium that employs synchronous technologies such as SONET/SDH. Similar to the utilization of faster transmission rates over copper wire, SONET/SDH protocols such as OC-3 (155Mbps) and OC-12 (622Mbps) are being upgraded to OC-48 (2.5Gbps) and OC-192 (10Gbps) to increase the bandwidth over optical fiber.

Exar's analog and mixed-signal design expertise, combined with its systems understanding, enables the Company to provide physical interface and access control solutions for WAN communications equipment. Exar currently offers ICs based upon the T/E carrier and ATM transmission standards and has introduced its first product based upon the SONET/SDH transmission standards. Exar's products offer its customers the following benefits:

- increased bandwidth through the integration of multiple channels on a single device
- reduced system noise/jitter to improve data integrity
- reduced overall system cost through the integration of multiple functions on a single device
- accelerated time-to-market by allowing them to focus on core competencies and outsource standards-based solutions.

Key elements of Exar's solution include:

Leading Analog and Mixed-Signal Design Expertise. The Company has 30 years of experience in developing analog and mixed-signal ICs. As a result, it has developed a significant knowledge base in these areas and a library of design elements. For example, Exar has particularly strong expertise in the design of high-speed, low-jitter phase lock loops, which are key elements in its mixed-signal transceiver products. As a result, Exar can provide its customers with products that typically exceed standard specifications and allow them flexibility in designing other system elements.

Broad Product Offerings. Exar offers a variety of physical interface and access control products based upon the T1/E1, T3/E3, ATM, and SONET/SDH transmission standards. Exar's broad multi-channel, multi-function portfolio for each transmission standard enables its customers to minimize board space and overall cost in

multi-port applications. Exar also offers a diverse portfolio of both industry standard and proprietary UARTs (universal asynchronous receiver transmitters).

Comprehensive Solutions to Enhance System Integration. The combination of Exar's design and system level expertise allows it to provide a comprehensive solution that encompasses hardware, software and applications support. Using Exar's solutions, OEMs can efficiently integrate the Company's devices into their systems, better leverage their development resources and reduce their time-to-market.

Compelling Price/Performance Solutions. Exar uses its systems expertise and its analog, digital and mixed-signal design techniques to architect high-performance products based on standard CMOS process technologies. These CMOS processes are proven, stable, predictable and able to meet the application speed and power/performance requirements at a lower price point than other semiconductor manufacturing processes.

Video and Imaging Markets and Exar's Solution

The video market is composed of several segments, including digital still cameras, or DSCs, PC video cameras, security cameras, camcorders and digital camcorders. Among these applications, one of the fastest growing segments is DSCs. To create images that are more comparable to film cameras and include features such as steady-shot and digital zoom, DSCs and digital camcorders are requiring higher resolution and higher speed data acquisition subsystems, also known as analog front ends, or AFEs, and analog-to-digital converters, or ADCs.

Exar supplies high-performance ADCs and integrated AFEs that provide signal conditioning and digitization of charged couple device (CCD) signals. These ICs are used in products such as DSCs, digital copiers, scanners and multifunctional peripherals, or MFPs, which incorporate scanning, faxing and copying functions in a single integrated system. The Company uses advanced design techniques and process technologies to integrate low-power converter architectures with surrounding analog functions, reducing total system cost.

Products

Exar designs, develops and markets high-performance, high-bandwidth, physical interface and access control solutions for the worldwide communications infrastructure. The Company's current IC products for the communications market are designed to respond to the growing demand for high-speed networking equipment based on transmission standards such as T/E carrier, ATM and SONET/SDH. Exar also designs, develops and markets IC products that address the needs of the serial communications market and the video and imaging markets. Exar uses its design methodologies to develop products ranging from application specific standard products, or ASSPs, designed for industry-wide applications, to semi-custom solutions for specific customer applications. These complementary products enable the Company to offer a range of solutions for its customers' applications.

Communications

Exar's products for T/E carrier, ATM and SONET/SDH applications include high-speed analog, digital and mixed-signal physical interface and access control ICs. The physical interface ICs consist of a transmitter and receiver that, when integrated, is called a transceiver chip. Transceivers interface with the physical transmission media. Most of these high-speed, mixed-signal ICs convert parallel digital inputs into a single analog bit stream that is up to 32 times faster than the original signal. Access control circuits are digital circuits that format, or frame, the data and perform error checking.

Exar's communications products include transmitters and receivers, transceivers, jitter attenuators, framers, ATM user network interfaces, or ATM UNIs, and an M13 multiplexer. These products are used in SONET/SDH multiplexers, private branch exchanges (PBX), central office switches and digital cross connects. Exar maintains a dominant market position in T3/E3/STS-1 transceivers. As of September 2001, this transceiver family had 150 design wins. Exar has extended this transceiver family with integrated jitter attenuator functionality. Exar's access control products include framers, ATM UNI/PPP and an M13 multiplexer. These newer products are achieving greater market acceptance as the Company's strong transceiver products have allowed it to compete for adjacent component opportunities. During the third calendar quarter, Exar announced its first data aggregation product opening new opportunities for the Company in the metro market. First in a planned family, this device can aggregate 12 channels of T3/E3/STS-1onto an OC-12/STM-4 data stream. Exar also supplies a family of V.35 transceiver and multiprotocol products used for high-speed data transmission, primarily in networking equipment such as routers and bridges.

The Company expects to introduce a number of new communication ICs in the current fiscal year to provide an expanded line of T/E carrier products as well as SONET/SDH products. The T/E carrier products are expected to include multi-channel, multi-function ICs that integrate transceivers, jitter attenuators, framers and ATM UNIs. SONET/SDH product introductions are expected to focus on data aggregation combining T3/E3 capability with OC-3 (155 Mbps) and OC-12 (622 Mbps) functions.

Serial Communications

UARTs convert data streams from parallel to serial, enabling a serial data stream to communicate with a central processing unit, or CPU. Exar sells its UART products to the remote access, data collection, industrial automation and handheld/mobile markets. Many of these products include high performance features, such as automated flow control and large First-In First-Out, or FIFO, buffers. Exar has designed a highly integrated quad, or four-channel, UART with FIFO circuitry, which the Company believes is the de facto industry standard for quad FIFO UARTs used in multi-channel networking applications. During the current fiscal year, Exar expects to expand its family of PCI multi-channel UARTs.

Video and Imaging

As previously stated, the video market is composed of several segments, including DSCs (digital still cameras), PC video cameras, security cameras, camcorders and digital camcorders which require higher resolution and higher speed data acquisition subsystems. These subsystems encompass AFEs (analog front ends) and ADCs (analog-to-digital converters).

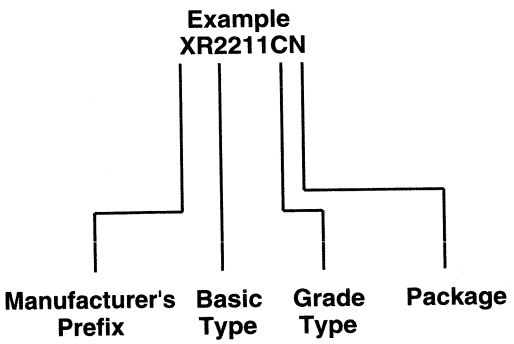
Exar supplies integrated, high-performance subsystems, as well as, ADCs and DACs (digital-to-analog converters) for products such as DSCs, digital camcorders, scanners and MFPs (multifunctional peripherals) which incorporate scanning, faxing and copying functions in a single integrated system. The Company uses advanced design techniques and process technologies to integrate low-power converter architectures with surrounding analog functions, reducing total system cost.

Manufacturing and Quality

Exar is a fabless semiconductor supplier utilizing industry leading foundries for its manufacturing requirements. Although, Exar offers products in a variety of bipolar, CMOS and BiCMOS processes, the majority of its products are produced in CMOS. The Company offers its products in a wide selection of surface mount and through-hole packages. Exar's primary wafer manufacturer is Chartered Semiconductor. Contract assembly and test suppliers include AIT, ASAT, Carsem and STATs. Exar is a charter member of the Fabless Semiconductor Association (FSA) and a member of the American Electronics Association (AEA).

The Company is ISO 9001 and QS-9000 certified, and has a Total Quality Management system based on continual quality improvement that is focused on the goals of customer satisfaction, streamlined business processes, and leverage of development resources.

PRODUCT ORDERING INFORMATION
(PRODUCT INTRODUCED PRIOR TO 1990)



Grade

M = Military
N = Prime Electrical
P = Prime Electrical
C = Commercial
I = -40°C to +85°C

N, P, CN and CP parts are electrically identical and operate over 0°C to +70°C unless otherwise stated. In addition, N and P parts generally have operating parameters more tightly controlled than the CN or CP parts

Package Suffix:

N = Ceramic Dual-in-Line
P = Plastic Dual-in-Line
D = Plastic Jedec SOIC*
L = Leadless Chip Carrier*
J = Plastic Leaded Chips (J lead) (PLCC)*
Q = Quad Pack-Gullwing*
MD = Plastic Japanese SOIC*
DIE = Individual Dice in Waffle Pack**
F = Wafer**
H = Hybrid
V = Shrink Quad Flat Pack*
W = SOJ*

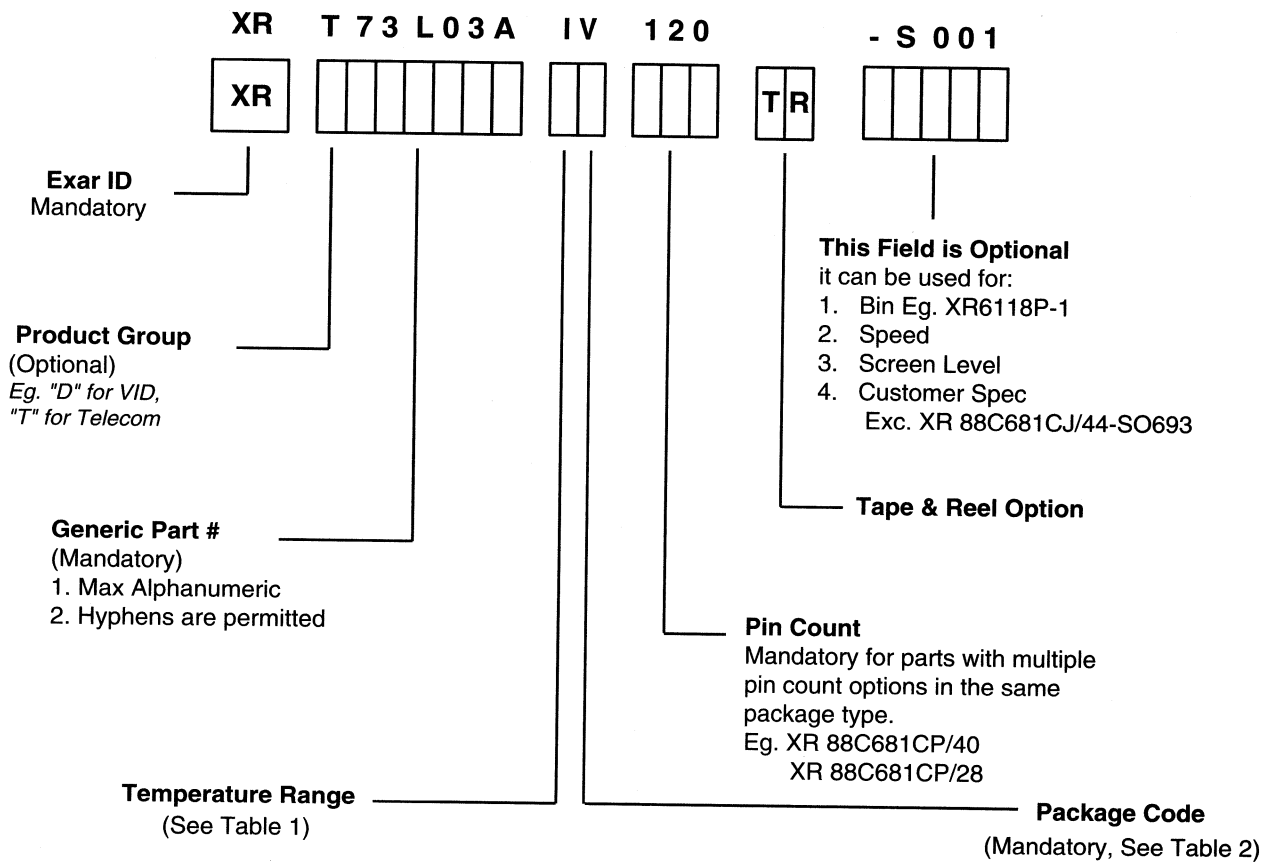
* Surface Mount Packages
** Not Available Through Distribution

Notes:

1. Minimum line item value is $500.00 U.S.
2. Specially screened products do not fall under standard terms and conditions.

PRODUCT ORDERING INFORMATION
(FOR PRODUCTS INTRODUCED IN AND SINCE 1990)

EXAMPLE



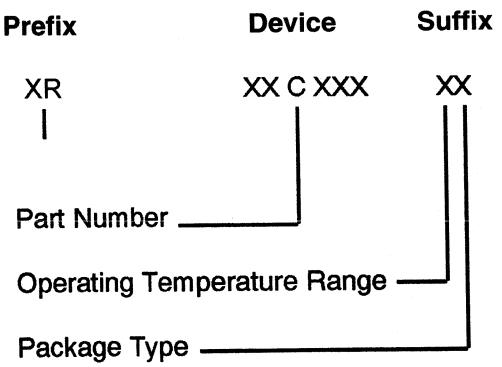
Suffix	Description
C	0°C to +70°C
I	-40°C to +85°C
M	-55°C to +125°C
W	As specified on datasheet

Table 1. Temperature Range

Suffix	Description
B	BGA, Ball Grid Array
C	Die (Chip)
D	SOIC, JEDEC Plastic Small Outline
G	TSSOP, Thin Shrink SOP
J	PLCC, Plastic Lead Carrier
K	SOP, EIAJ, Plastic Small Outline
L	LCC, Ceramic, Leadless Chip Carrier
M	TQFP, Thin QFP, package thickness1.0mm or less
N	CDIP, Ceramic Dual In Line
P	PDIP, Plastic Dual In Line
Q	QFP, Plastic Quad Flat Pack (Matric QFP or MQFP)
U	SSOP, Plastic Shrink SOP
V	SQFP, Plastic Shrink QFP, JEDEC 1.4mm thick TQFP
W	SOJ, JEDEC Plastic J-Lead Small Outline

Table 2. Package Designator Description

PACKAGE MARKING INFORMATION
EXCEPT TIMING PRODUCTS



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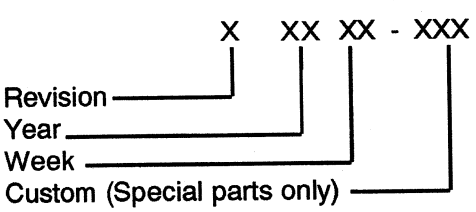
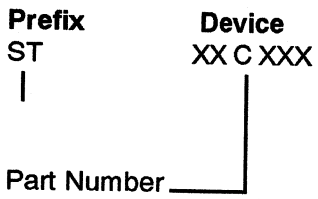


PACKAGE MARKING INFORMATION
TIMING PRODUCTS

14-Lead SOIC



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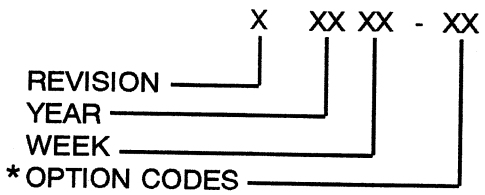
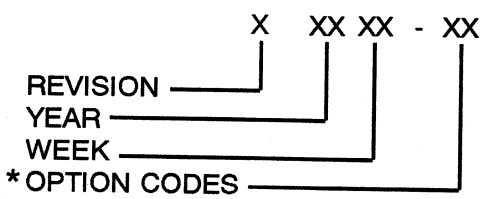


8-Lead SOIC

Prefix	Device
ST	XXXX

DATE CODE AND OPTIONS MARKING



EXAR

GENERAL INFORMATION

COMMUNICATIONS PRODUCTS

WORLDWIDE SALES OFFICES

PCM and DS1/E1 Products

Part Number	No. of Channels	Data Rates	Clock Recovery	Short/Long Haul	Temp Range	Operating Power Supply, and Max Current		Package(s)
						V_{DD}	I_{DD}	
Line Interfaces								
XRT5793	4	E1	No	S	-40°C to +85°C	±5V ±5%	68mA	80-TQFP, 68-PLCC
XRT5794	4	E1	No	S	-40°C to +85°C	±5V ±5%	68mA	80-TQFP, 68-PLCC
XRT5894	4	E1	No	S	-40°C to +85°C	3.3V, 5V ±5%	210mA	64-TQFP
XRT5897	7	E1	No	S	-40°C to +85°C	3.3V, ±5%,	340mA	100-TQFP
XRT59L91	1	E1	No	S	-40°C to +85°C	3.3V ±5%	56mA	16-SOIC
XRT5997	7	E1	No	S	-40°C to +85°C	3.3V ±5%	175mA	100-TQFP
XRT7288	1	E1	Yes	S	-40°C to +85°C	5V ±10%	53mA	28-SOJ, 28-PDIP
XRT81L27	7	E1	Yes	S	-40°C to +85°C	3.3V ±5%	180mA	128-TQFP
XRT82D20	1	E1	Yes	S	-40°C to +85°C	3.3V, 5V ±5%	58mA	28-SOJ
XRT82L24	4	E1	Yes	S	-40°C to +85°C	3.3V ±5%	228mA	100-TQFP
XRT82L34	4	T1/E1	Yes	S	-40°C to +85°C	3.3V ±5%	TBD	100-TQFP
XRT82L38	8	T1/E1	Yes	S	-40°C to +85°C	3.3V ±5%	TBD	144-TQFP
XRT83L30	1	T1/E1/J1	Yes	S/L	-40°C to +85°C	3.3V ±5%	TBD	64-TQFP
XRT83L34	4	T1/E1/J1	Yes	S/L	-40°C to +85°C	3.3V ±5%	TBD	128-TQFP
XRT83L38	8	T1/E1/J1	Yes	S/L	-40°C to +85°C	3.3V ±5%	TBD	208-TQFP
PCM Line Interfaces								
XRT5683A	1	T1/E1/T2/E2	Yes, w/ Tank Ckt	S	-40°C to +85°C	5V ±5%	40mA	18-PDIP, 18-SOIC
XRT56L85	1	E1	Yes, w/ Tank Ckt	S	-40°C to +85°C	5V ±5%	16mA	18-SOIC, 18-CDIP
Framers								
XRT84L14	4	T1	N/A	N/A	-40°C to +85°C	3.3V ±5%	40mA	208-PQFP
XRT84L18	8	T1	N/A	N/A	-40°C to +85°C	3.3V ±5%	16mA	388-BGA
XRT84V24	4	E1	N/A	N/A	-40°C to +85°C	3.3V ±5%	TBD	208-PQFP
XRT84L38	8	T1/E1/J1	N/A	N/A	-40°C to +85°C	3.3V ±5%	TBD	388-BGA

Clock Adapter

Part Number	No. PLLs	Input Frequency Range	Output Frequency Range	Temp. Range	Operating Power Supply V_{DD}	Package(s)
XRT8000	2	8kHz to 32,768kHz	150Hz to 2,048kHz	-40°C to +85°C	3.3V, 5.0V	18–PDIP, 18–SOIC
XRT8001	2	8kHz to 32,768kHz	56kHz to 16,384kHz	-40°C to +85°C	3.3V, 5.0V	18–PDIP, 18–SOIC

DS3/E3/STS-1 Products

Part Number	No. of Channels	Data Rates	Clock Recovery	Temp Range	Operating Power Supply, Max Current		Package(s)
					V_{DD}	I_{DD}	
Line Interface							
XRT7295 (Receiver)	1	DS3, STS-1	Yes	-40°C to +85°C	5V ±5%	111mA	20-SOJ, 20-PDIP
XRT7295AT (Receiver)	1	DS3, STS-1	Yes	-40°C to +85°C	5V ±5%	111mA	20-SOJ
XRT7295E (Receiver)	1	E3	Yes	-40°C to +85°C	5V ±5%	106mA	20-SOJ, 20-PDIP
XRT7295AE (Receiver)	1	E3	Yes	-40°C to +85°C	5V ±5%	106mA	20-SOJ
XRT7296 (Transmitter)	1	DS3, E3, STS-1	N/A	-40°C to +85°C	5V ±5%	133mA	28-SOJ, 28-PDIP
XRT7298 (Transmitter)	1	DS3, E3, STS-1	N/A	-40°C to +85°C	5V ±5%	133mA	28-SOJ, 28-PDIP
XRT7300	1	DS3, E3, STS-1	Yes	-40°C to +85°C	5V ±5%	220mA	44-TQFP
XRT73L00A	1	DS3, E3, STS-1	Yes	-40°C to +85°C	3.3V ±5%	150mA	44-TQFP
XRT7302	2	DS3, E3, STS-1	Yes	-40°C to +85°C	5V ±5%	440mA	80-TQFP
XRT73L02A	2	DS3, E3, STS-1	Yes	-40°C to +85°C	3.3V ±5%	350mA	80-TQFP
XRT73L03A	3	DS3, E3, STS-1	Yes	-40°C to +85°C	3.3V ±5%	370mA	120-TQFP
XRT73L04A	4	DS3, E3, STS-1	Yes	-40°C to +85°C	3.3V ±5%	550mA	144-TQFP
DS3/E3/STS-1 Jitter Attenuator							
XRT71D00	1	DS3, E3, STS-1	N/A	-40°C to +85°C	3.3V, 5V ±5%	65mA	32-TQFP
XRT71D03	3	DS3, E3, STS-1	N/A	-40°C to +85°C	3.3V, 5V ±5%	120mA	64-TQFP
XRT71D04	4	DS3, E3, STS-1	N/A	-40°C to +85°C	3.3V, 5V ±5%	130mA	80-TQFP
DS3/E3/STS-1 Integrated Lin Interface Unit and Jitter Attenuator							
XRT75L03	3	DS3, E3, STS-1	Yes	-40°C to +85°C	3.3V ±5%	460mA	128-TQFP
DS3/E3 Framer							
XRT7250	1	DS3, E3	N/A	-40°C to +85°C	5V ±5%	150mA	100-PQFP
XRT72L50	1	DS3, E3	N/A	-40°C to +85°C	3.3V ±5%	50mA	100-PQFP
XRT72L52	2	DS3, E3	N/A	-40°C to +85°C	3.3V ±5%	150mA	160-PQFP
XRT72L53	3	DS3, E3	N/A	-40°C to +85°C	3.3V ±5%	230mA	272-BGA
XRT72L54	4	DS3, E3	N/A	-40°C to +85°C	3.3V ±5%	300mA	272-BGA
XRT72L56	6	DS3, E3	N/A	-40°C to +85°C	3.3V ±5%	375mA	388-BGA
XRT72L58	8	DS3, E3	N/A	-40°C to +85°C	3.3V ±5%	450mA	388-BGA
M13 Multiplexer							
XRT72L13	1	DS3	N/A	-40°C to +85°C	3.3V ±5%	220mA	208-PQFP

ATM Products

Part Number	No. of Channels	Description	Temp. Range	Operating Power Supply	Package(s)
XRT7234 (1)	1	E3 UNI	-40°C to +85°	5.0V ±10%	160-PQFP
XRT7245	1	DS3 UNI	-40°C to +85°	5.0V ±10%	160-PQFP
XRT72L71 (1)	1	DS3 UNI	-40°C to +85°	3.3V ±10%	160-PQFP
XRT72L73 (1)	3	DS3 UNI	-40°C to +85°	3.3V ±10%	352-PBGA
XRT72L74 (1)	4	DS3 UNI	-40°C to +85°	3.3V ±10%	352-PBGA
XRT74L73(1)	3	DS3/E3 UNI	-40°C to +85°	3.3V ±5%	388-PBGA
XRT74L74(1)	4	DS3/E3 UNI	-40°C to +85°	3.3V ±5%	388-PBGA

Note:
(1) Preliminary

SONET/SDH

Part Number	Data Rate	Protocols	Transceiver Bus I/F	System Bus I/F	Power Supply	Package(s)
XRT94L43	1 STS-12/STM-4 4 x STS-3/STM-1 12 x DS3/E3/STS-1	POS	8-bit 77.76MHz	POS-PHY	2.5V	516-PBGA
XRT95L51	1 x STS-48 4 x STS-12	ATM, POS	16-Bit, 155.52MHz	Utopia Level 3, 32-Bit, 100MHz	3.3V ± 5%	388-PBGA

Co-Directional Products

Part Number	No. of Channels	Data Rates	Clock Recovery	Short/Long Haul	Temp Range	Operating Power Supply, Max Current		Package(s)
						V_{DD}	I_{DD}	
XRT6164 (1)	1	64Kbps, E1	No	S	0°C to +70°C	5V ±5%	26.5mA	16-SOIC, 16-PDIP
XRT6164A (2)	1	64Kbps, E1	No	S	-10°C to +85°C	5V ±5%	26.5mA	16-SOIC, 16-PDIP
XRT6165 (3)	1	64Kbps, E1	Yes	N/A	0°C to +70°C/ -40°C to +85°C	5V ±10%	2mA	24-SOIC, 22-PDIP
XRT6166 (4)	1	64Kbps, E1	Yes	N/A	0°C to +70°C/ -40°C to +85°C	5V ±10%	2mA	28-SOIC, 28-PDIP

Notes:
(1) 64Kbps Co-directional Line Interface Unit, when used with XRT6165 or XRT6166.
(2) XRT6164A is the Ind. Temp. Grade of XRT6164.
(3) Co-directional Digital Data Processor.
(4) Co-directional Digital Data Processor with Slip Buffer.

Network Interface Products

Part Number	No. of Drivers	No. of Receivers	Control Logic	Control Type	Temp. Range	Max Speed	Package(s)
RS422/RS423 Interfaces							
ST26C31	4		1	"OR-ed"	0°C to +70°C/ -40°C to +85°C	10MHz	PDIP-16, SOIC-16
ST26C32		4	1	"OR-ed"	0°C to +70°C/ -40°C to +85°C	10MHz	PDIP-16, SOIC-16
ST34C86		4	2	Active High	0°C to +70°C/ -40°C to +85°C	10MHz	PDIP-16, SOIC-16
ST34C87	4		2	Active High	0°C to +70°C/ -40°C to +85°C	10MHz	PDIP-16, SOIC-16

Part Number	No. of Rec.	No. of Trans.	Loop-back	RCV V.11	Supplies	Max Speed	Temp. Range	XMT Disable	Disable	Max Power	Max Shutdown Current	Package(s)
V.35 Interfaces												
XRT3588		3	No	No	+5, -5	10 Mbps	0°C to +70°C	Yes	N/A	1280mW	10.2mA	18-PDIP, 18-CDIP
XRT3589	3		No	No	+5, -5	10 Mbps	0°C to +70°C	N/A	Yes	345mW	1.1mA	14-CDIP
XRT3590	3	3	Yes	Yes	+5, -5	20 Mbps	-40° to +85°C	Yes	Yes	600mW	300µA	24-PDIP, 24-SOIC
XRT3591B	3	3	Yes	Yes	+5, -5	20 Mbps	-40° to +85°C	Yes	Yes	600mW	300µA	24-PDIP, 24-SOIC
Universal Serial Interfaces												
XRT4500 (1)	8	8	Yes	Yes	5	20 Mbps	0° to 70°C	Yes	Yes	2000mW	110mA	80-TQFP

Note: (1) Receivers and transmitters support multiple interfaces such as V.35, RS232, RS449, EIA 530 (A), X.21, V.36.

General Purpose Timing Products

Part Number	Max Speed	Max Current	Package(s)
ST49C101A	200MHz	3.3V, 5V	8-SOIC
ST49C107A	130MHz	5V	14-SOIC
Phase Lock Loop (PPL)			
Part Number	**Frequency**	**Max Current**	**Package(s)**
XR215A	0.01Hz to 300KHz	4.5V to 20V	16-CDIP, 16-PDIP
XR2212	0.5Hz to 25KHz	5V to 26V	16-CDIP, 16-PDIP
FSK Demodulator/Tone Decoder			
XR2211	0.01Hz to 300KHz	4.5V to 20V	14-CDIP, 14-PDIP, 14-SOIC
XR2211A	0.5Hz to 25KHz	5V to 26V	14-PDIP, 14-SOIC
Voltage Controlled Oscillator			
XR2207	0.01Hz to 1MHz	4V to 13V	14-CDIP, 14-PDIP, 16-SOIC
XR2209	0.01Hz to 1MHz	4V to 13V	8-PDIP, 8-CDIP
Voltage to Frequency Converter			
Part Number	**Internal Power Dissipation**	**Max Current**	**Package(s)**
XR4151	500mW	8V to 22V	8-PDIP, 8-SOIC
Function/Waveform Generators			
Part Number	**Sweep Range**	**Max Current**	**Package(s)**
XR2206	2000:1	10V to 26V	16-CDIP, 16-PDIP, 16-SOIC
XR8038A	-	36V	14-PDIP
Voice Switched Speakerphone			
Part Number	**Max Supply Voltage**	**Max Power Down Supply Current**	**Package(s)**
XRT65118A	6.5V	6.5mA	28-PDIP, 28-SOIC

For further information on these products, please use the CDROM catalog in the back of this book or go to Exar's web site at *www.exar.com.*

I/O Products

Part Number	Osc./Ext CLK	V_{CC} Volt	Typ. 1cc (mA)	Temp. Grade	Packages	Data Bus I/F	Other Features
ST78C34	Osc.	5	4	0°C to +70°C	PDIP-40, PLCC-44	Intel	Standard Centronics Printer Port (SPP) Host with 83-byte of FIFO and on-chip oscillator.
ST78C36	Ext. CLK	5	TBD	0°C to +70°C	PLCC-44, TQFP-64	Intel	SPP/ECP/EPP (IEEE 1284) Printer Port Host with 16-byte FIFO and printer port direction indicator. PLCC package provides Ext. Clock, 1 DMA & 1 interrupt (H/W select). TQFP package provides on-chip oscillator, 3 DMA & 1 interrupt (S/W select).
ST78C36A	Osc.	5	TBD	0°C to +70°C	PLCC-44	Intel	SPP/ECP/EPP (IEEE 1284) Printer Port Host with 16-byte FIFO, on-chip oscillator, 1 DMA & 1 interrupt (H/W select).

Serial Communications/UARTs

Part Number	Channels	Osc./ Ext CLK	Data Rate @ 5V/3.3 (Mbps)	TX/RX FIFO Bytes	TX & RX FIFO Counters	RX/TX FIFO INT Trigger	Auto RTS/ CTS	VCC Volt	Typ. ICC (mA)	Temp. Grade	Packages
ST16C1450	1	Osc.	1.5/0.5	0/0	No	No/No	No	+3.3, +5	1.2	C, I	PDIP-28, PLCC-28, TQFP-48
ST16C1451	1	Ext CLK	1.5/0.5	0/0	No	No/No	No	+3.3, +5	1.2	C, I	PDIP-28, PLCC-28, TQFP-48
ST16C1550	1	Osc.	1.5/0.5	16/16	No	4 Levels/ 4 Levels	No	+3.3, +5	1.2	C, I	PDIP-28, PLCC-28, TQFP-48
ST16C1551	1	Ext CLK	1.5/0.5	16/16	No	4 Levels/ 4 Levels	No	+3.3, +5	1.2	C, I	PDIP-28, PLCC-28, TQFP-48
ST16C450	1	Osc.	1.5/0.5	0/0	No	No/No	No	+3.3, +5	1.2	C, I	PDIP-40, PLCC-44, TQFP-48
ST16C550	1	Osc.	1.5/0.5	16/16	No	4 Levels/No	No	+3.3, +5	1.2	C, I	PDIP-40, PLCC-44, TQFP-48
ST16C580	1	Osc.	1.5/0.5	16/16	No	4 Levels/ 4 Levels	Yes	+3.3, +5	1.2	C, I	PDIP-40, PLCC-44, TQFP-48
ST16C650A	1	Osc.	1.5/0.5	32/32	No	4 Levels/ 4 Levels	Yes	+3.3, +5	1.2	C, I	PDIP-40, PLCC-44, TQFP-48
XR16L651	1	Osc.	3.0/2.0	32/32	No	4 Levels/ 4 Levels	Yes	+2.5, +3.3, +5	1.2	C, I	TQFP-48
XR16C850	1	Osc.	1.5/0.5	128/128	Yes	Program/ Program	Yes	+3.3, +5	1.3	C, I	PDIP-40, PLCC-44, TQFP-48, QFP-52
ST16C2450	2	Osc.	1.5/0.5	0/0	No	No/No	No	+3.3, +5	1.2	C, I	PDIP-40, PLCC-44, TQFP-48
ST16C2550	2	Osc.	4.0/2.0	16/16	No	4 Levels/No	No	+3.3, +5	1.2	C, I	PDIP-40, PLCC-44, TQFP-48
ST16C2552	2	Osc.	1.5/0.5	16/16	No	4 Levels/No	No	+3.3, +5	1.2	C, I	PLCC-44
XR16C2850	2	Osc.	1.5/0.5	128/128	Yes	Program/ Program	Yes	+3.3, +5	3	C, I	PDIP-40, PLCC-44, TQFP-48
XR16C2852	2	Osc.	1.5/0.5	128/128	Yes	Program/ Program	Yes	+3.3, +5	3	C, I	PLCC-44
ST16C452/ ST16C452PS	2	Ext CLK	1.5/0.5	0/0	No	No/No	No	+3.3, +5	1.2	C, I	PLCC-68

Note: *C = 0°C to +70°C*
I = -40°C to +85°C

Serial Communications/UARTs (Cont'd)

Part Number	Channels	Osc./ Ext CLK	Data Rate @ 5V/3.3 (Mbps)	TX/RX FIFO Bytes	TX & RX FIFO Counters	RX/TX FIFO INT Trigger	Auto RTS/ CTS	V_{CC} (Volt)	Typ. ICC (mA)	Temp. Grade	Packages
ST16C552/ ST16C552A	2	Ext CLK	1.5/0.5	16/16	No	4 Levels/No	No	+3.3, +5	1.2	C, I	PLCC-68
XR16C872	2	Osc.	460Kbps	128/128	Yes	Program/ Program	Yes	+3.3, +5	3	C, I	QFP-100
XR68C681	2	Osc.	1.0	1/3	No	No/No	Yes	+5	6	C, I	PLCC-44, PDIP-40, CDIP-40
XR88C681	2	Osc.	1.0	1/3	No	No/No	Yes	+5	6	C, I	PDIP-28, PLCC-44, PDIP-40, CDIP-40
XR68C92/ XR88C92	2	Osc.	1.0	8/8	No	Yes/Yes	Yes	+3.3, +5	1	C, I	PDIP-40, PLCC-44, TQFP-44
XR68C192/ XR88C192	2	Osc.	1.0	16/16	No	Yes/Yes	Yes	+3.3, +5	1	C, I	PDIP-40, PLCC-44, TQFP-44
ST16C454	4	Osc.	1.5/0.5	0/0	No	No/No	No	+3.3, +5	3	C, I	PLCC-68
ST16C554/ ST16C554D	4	Osc.	1.5/0.5	16/16	No	4 Levels/No	No	+3.3, +5	3	C, I	PLCC-68, TQFP-64
ST16C654/ ST16C654D	4	Osc.	1.5/0.5	64/64	No	4 Levels/ 4 Levels	Yes	+3.3, +5	6	C, I	PLCC-68, TQFP-64, QFP-100
XR16C854/ XR16C854D	4	Osc.	1.5/0.5	128/128	Yes	Program/ Program	Yes	+3.3, +5	6	C, I	PLCC-68, TQFP-64, QFP-100
XR16C864	4	Osc.	1.5/0.5	128/128	Yes	Program/ Program	Yes	+3.3, +5	6	C, I	QFP-100
XR16L784	4	Osc.	3.125/ 2.0	64/64	Yes	Program/ Program	Yes	+3.3, +5	5	C, I	TQFP-64
ST68C454	4	Osc.	1.5/0.5	0/0	No	No/No	No	+3.3, +5	3	C, I	PLCC-68
ST68C554	4	Osc.	1.5/0.5	16/16	No	4 Levels/No	No	+3.3, +5	3	C, I	PLCC-68
XR82C684	4	Osc.	1.0	3/3	No	No/No	Yes	+5	6	C, I	PLCC-44, PLCC-68
XR16L788 (XR16L758)	8	Osc.	3.125/ 2.0	64/64	Yes	Program/ Program	Yes	+3.3, +5	5	C, I	QFP-100
XR17C158, PCI Bus	8	Osc.	3.125	64/64	Yes	Program/ Program	Yes	+5	5	C, I	TQFP-144
XR17L154, PCI Bus	4	Osc.	3.125	64/64	Yes	Program/ Program	Yes	+5	5	C, I	TQFP-144

Exar offers seamless solutions from T1 to T3 that designers can use to implement silicon solutions for the physical layer of wide area networking equipment. These devices can make hardware design simpler while still meeting today's complex telecom standards. Included in this overview are examples of chipsets that can be designed into three applications: a DS3 and E3 Frame Relay, a DS1 to DS3 Multiplexer, and an 8-channel T1/E1 system. In addition to the examples shown here, Exar also has a family of three and four channel DS3/E3 ATM UNIs that when combined with Exar LIUs provide a complete solution for the ATM physical layer.

Frame Relay

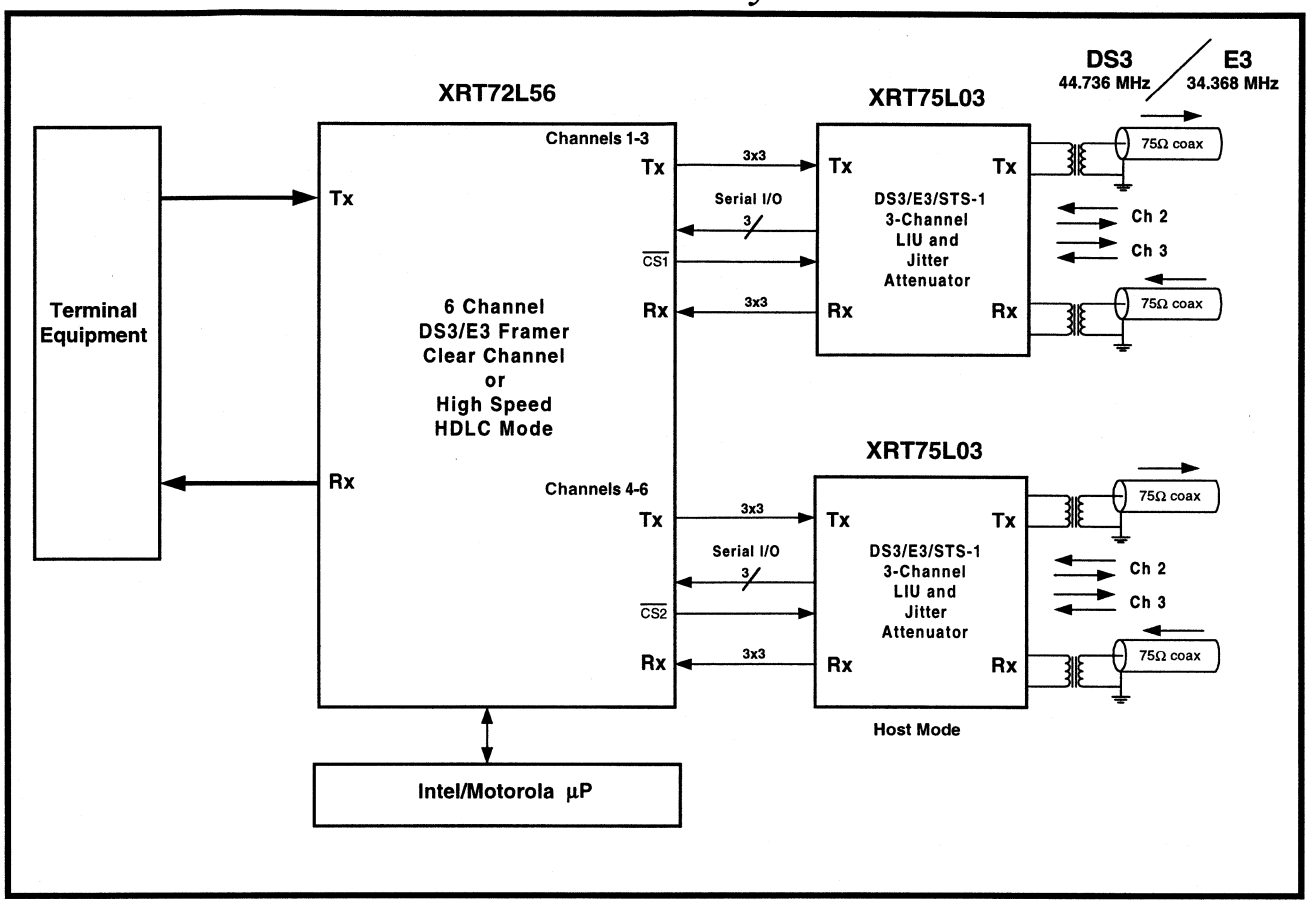


Figure 1. Six-channel DS3/E3 Clear Channel Framer with Two 3-channel DS3/E3/STS-1 LIUs and Jitter Attenuators

The XRT75L03 is the first multi-channel product to offer a line interface unit integrated with a jitter attenuator. This product offers the most complete solution available for the physical layer interface in a DS3/E3 system and it supports all of the relevant Bellcore and ITU standards covering, but not limited to, jitter transfer, jitter tolerance, intrinsic jitter, pulse template, and LOS detection. In addition, this product can support STS-1 rates and meets the standards for pulse templates and jitter for Bellcore TR-NWT-000253. Each channel of the XRT75L03 can be configured for an individual data rate allowing the part to support multiple data rates at the same time.

The XRT72L56 integrates six E3/DS3 clear channel framers in one package. These framers support ITU-T G.751 and ITU-T G.832 framing formats for E3 as well as M13 and C-bit parity framing formats for DS3. In addition, the XRT72L56 has six HDLC controllers in both the transmit and receive paths allowing Frame Relay to be implemented with just three ICs. There are also 1, 2, 3, 4 and 8-channel members of this clear channel DS3/E3 framer family.

When the XRT72L56 and XRT75L03 are combined, these products can directly talk to each other, offering a seamless connection between the line transformers and the higher level ASICs, or network processor in the system.

Multiplexer

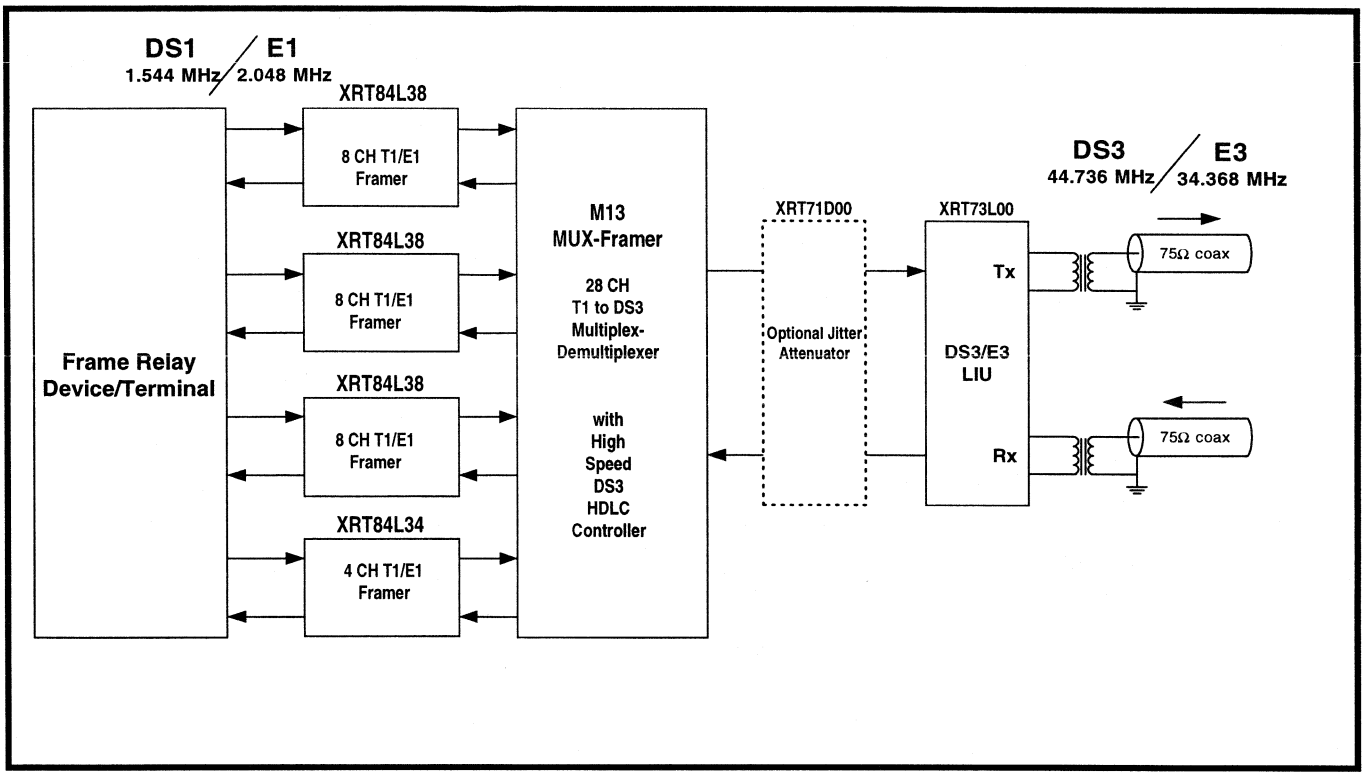


Figure 2. DS3-to-DS1 Multiplexer Using Eight and Four-Channel T1/E1 Framers, an M13 Multiplexer, a Jitter Attenuator and a LIU

Using discrete components, the XRT73L00 and the XRT71D00 deliver the implementation of one of the channels filled by the XRT75L03 that was shown in Figure 1. For designers who do not require a jitter attenuator in their system, the XRT73L00 alone offers a complete solution for the physical interface. There are also available 2, 3 and 4-channel versions of the XRT73L00, as well as 3 and 4-channel versions of the XRT71D00.

The XRT72L13 supports multiplexing of the DS3 frame to 28 DS1 channels. It can also support, through G.707, the multiplexing of a T3 to 21 E1 channels. Each of these channels can either be:

- transported through the backplane to another M13 multiplexer
- sent through a T1/E1 LIU, such as the XRT82L38, eight-channel T1/E1 Short Haul LIU, to another piece of equipment or to a group of T1/E1 framers, such as the XRT84L34 and XRT84L38, where the T1 frames can be deframed into 672 DS0 voice channels.

The XRT72L13 provides a gapped clock, simplifying clocking for the framer, and a clear channel framer mode (including an HDLC controller), allowing different protocols to be supported in the same equipment.

Clear-Channel Framing

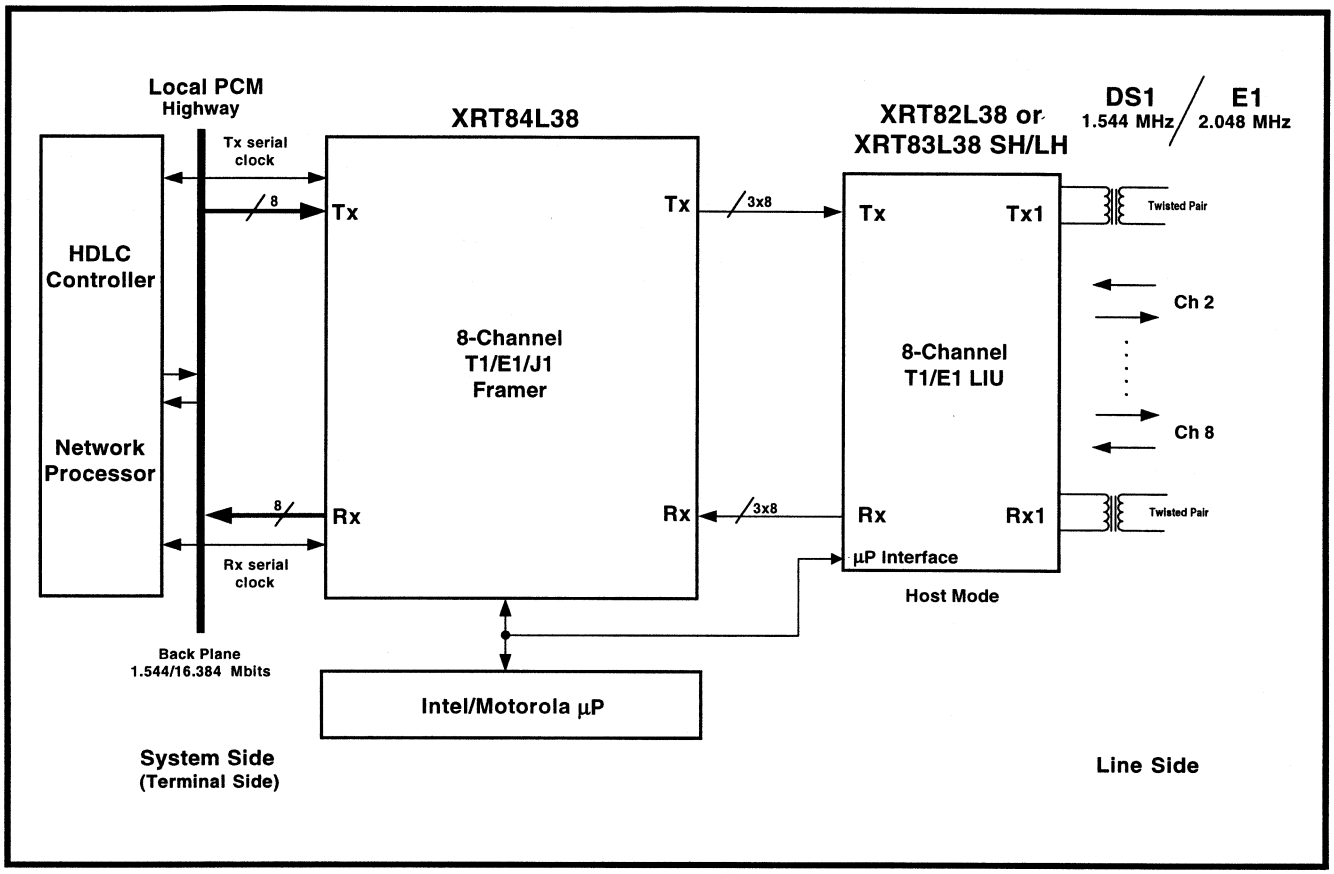


Figure 3. Eight-Channel T1 System Using an Eight-Channel LIU and an Eight-Channel Framer

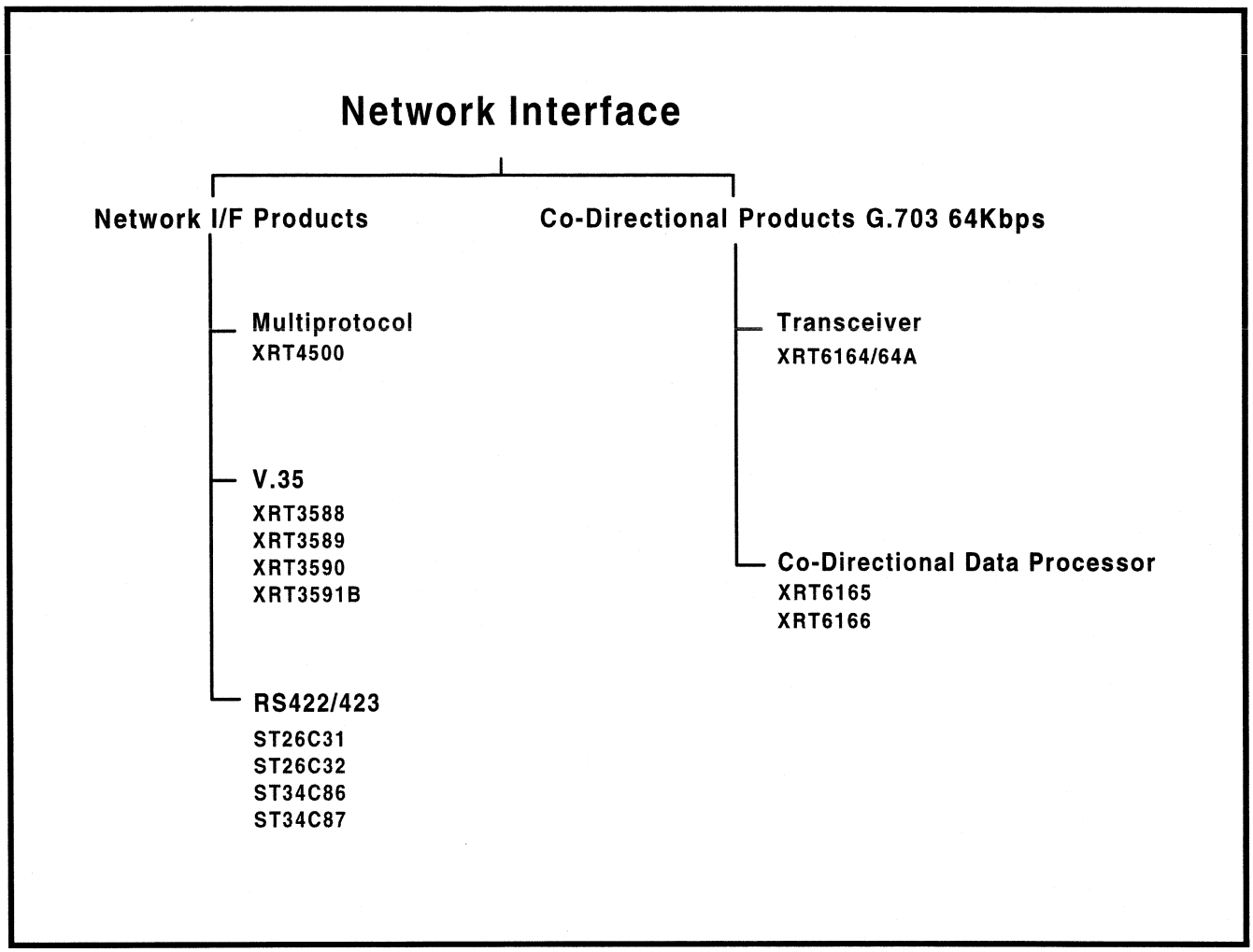
The XRT82L38 is an eight-channel short haul T1/E1 line interface unit that can be seamlessly interfaced to the XRT84L38, an eight-channel T1/E1 framer, to create a physical layer solution. This system can take DS0s though the local PCM highway and frame them into T1 or E1 frames and then transmit them over a twisted pair.

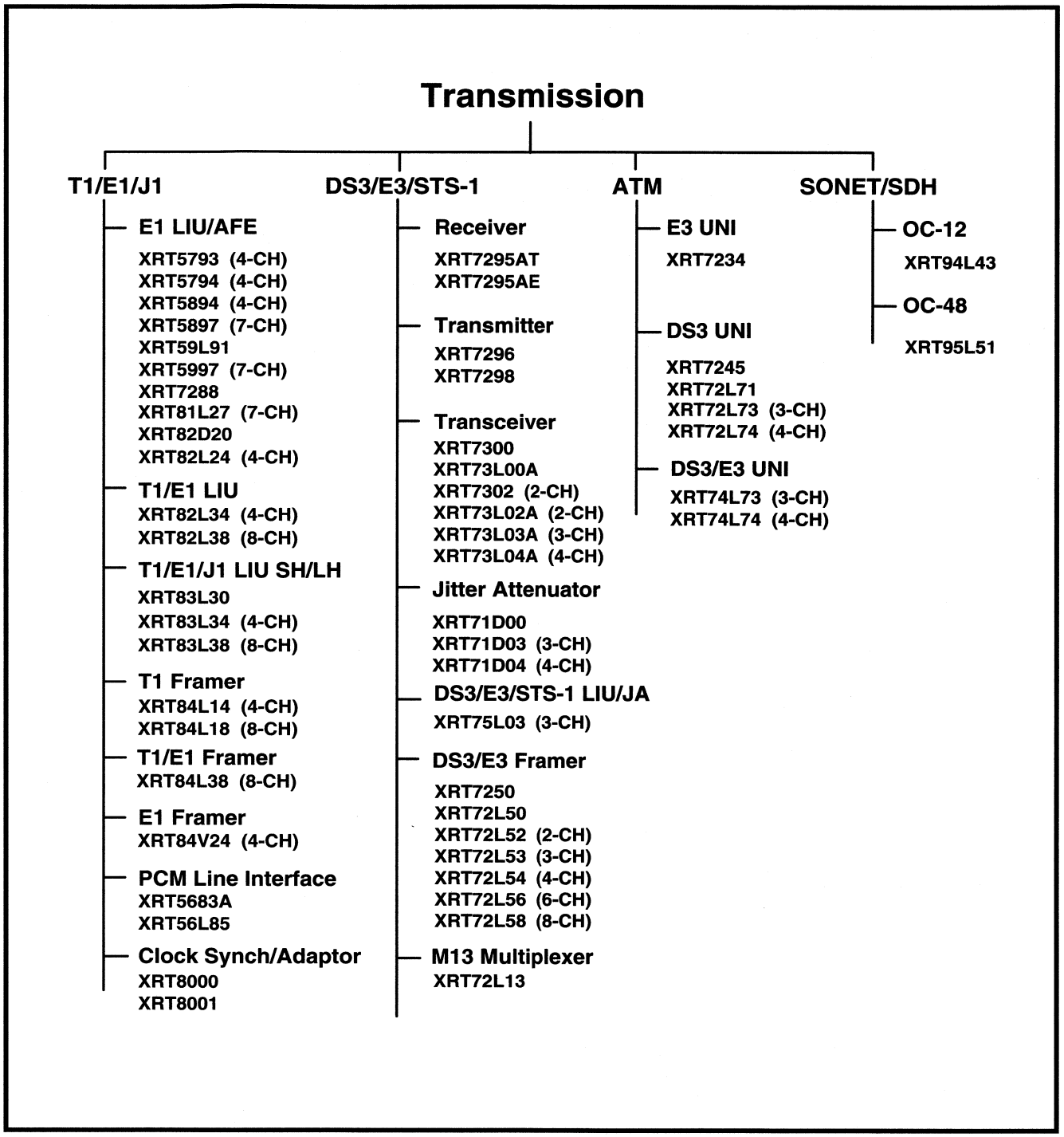
The framer supports all of the standard T1 and E1 framing formats, including Superframe, Extended Superframe, T1DM and SLIC-96 for T1, Common Channel Signaling, Frame Associated Signaling, and Channel Associated Signaling for E1. Each framer has two HLDC controllers for handling LAP-D protocol messaging to support network management.

The SH/LH LIU covers all the common T1 and E1 line impedances, 75, 100 and 120 Ohms. It also includes a jitter attenuator for each channel which can be selected for the transmit or receive path. Each channel contains an encoder/decoder for B8ZS and HDB3.

The microprocessor can control both parts through the parallel bus for configuration and network management. For applications requiring fewer channels, there is also a four channel device available.

Network Interface Tree




Transmission
T1/E1/J1
E1 LIU/AFE
XRT5793 (4-CH)
XRT5794 (4-CH)
XRT5894 (4-CH)
XRT5897 (7-CH)
XRT59L91
XRT5997 (7-CH)
XRT7288
XRT81L27 (7-CH)
XRT82D20
XRT82L24 (4-CH)
T1/E1 LIU
XRT82L34 (4-CH)
XRT82L38 (8-CH)
T1/E1/J1 LIU SH/LH
XRT83L30
XRT83L34 (4-CH)
XRT83L38 (8-CH)
T1 Framer
XRT84L14 (4-CH)
XRT84L18 (8-CH)
T1/E1 Framer
XRT84L38 (8-CH)
E1 Framer
XRT84V24 (4-CH)
PCM Line Interface
XRT5683A
XRT56L85
Clock Synch/Adaptor
XRT8000
XRT8001
DS3/E3/STS-1
Receiver
XRT7295AT
XRT7295AE
Transmitter
XRT7296
XRT7298
Transceiver
XRT7300
XRT73L00A
XRT7302 (2-CH)
XRT73L02A (2-CH)
XRT73L03A (3-CH)
XRT73L04A (4-CH)
Jitter Attenuator
XRT71D00
XRT71D03 (3-CH)
XRT71D04 (4-CH)
DS3/E3/STS-1 LIU/JA
XRT75L03 (3-CH)
DS3/E3 Framer
XRT7250
XRT72L50
XRT72L52 (2-CH)
XRT72L53 (3-CH)
XRT72L54 (4-CH)
XRT72L56 (6-CH)
XRT72L58 (8-CH)
M13 Multiplexer
XRT72L13
ATM
E3 UNI
XRT7234
DS3 UNI
XRT7245
XRT72L71
XRT72L73 (3-CH)
XRT72L74 (4-CH)
DS3/E3 UNI
XRT74L73 (3-CH)
XRT74L74 (4-CH)
SONET/SDH
OC-12
XRT94L43
OC-48
XRT95L51

QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

GENERAL DESCRIPTION

The ST26C31 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals, special hysteresis is built in the ST26C31 circuit.

The ST26C31 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST26C31 is suitable for low power 5V operation with high input voltage protection devices.

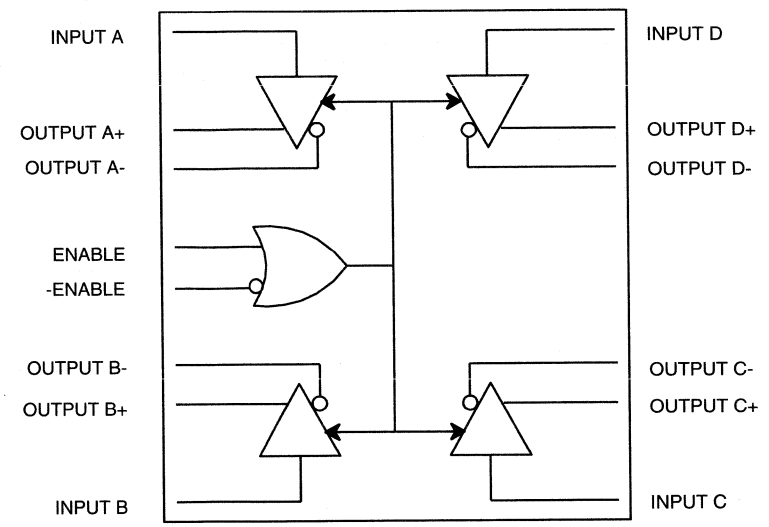
FEATURES

- Pin-to-Pin Compatible with National DS26C31C
- Low Power CMOS Design
- Three-State Outputs with Enable Pin
- Meets the EIA RS-422 Requirements
- Low Propagation Delays
- High Speed

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
ST26C31CP16	16-Lead 300 Mil PDIP	0°C to +70°C
ST26C31CF16	16-Lead 150 Mil JEDEC SOIC	0°C to +70°C
ST26C31IP16	16-Lead 300 Mil PDIP	-40°C to +85°C
ST26C31IF16	16-Lead 150 Mil JEDEC SOIC	-40°C to +85°C

ST26C31 BLOCK DIAGRAM



QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

REV. 1.01

GENERAL DESCRIPTION

The ST26C32 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST26C32 has an input sensitivity of 200mv over the common mode input voltage range of +7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST26C32 circuit.

The ST26C32 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422, and RS-423 differential applications. ST26C32 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST26C32 is suitable for low power 5V operation.

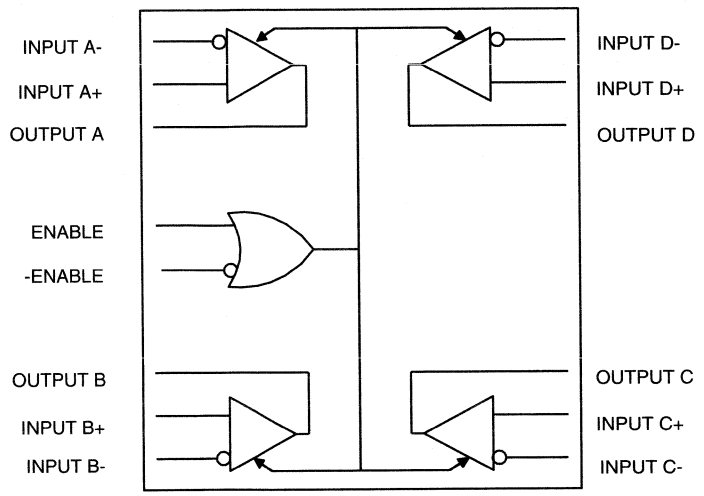
FEATURES

- Pin-to-Pin Compatible with National DS26C32C
- Low Power CMOS Design
- Three-State Outputs with Enable Pin
- Meets the EIA RS-422 Requirements
- Low Propagation Delays
- High Speed

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
ST26C32CP16	16-Lead 300 Mil PDIP	0°C to +70°C
ST26C32CF16	16-Lead 150 Mil JEDEC SOIC	0°C to +70°C
ST26C32IP16	16-Lead 300 Mil PDIP	-40°C to +85°C
ST26C32IF16	16-Lead 150 Mil JEDEC SOIC	-40°C to +85°C

ST26C32 BLOCK DIAGRAM



QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

REV. 1.01

GENERAL DESCRIPTION

The ST34C86 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST34C86 has an input sensitivity of 200mv over the common mode input voltage range of 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C86 circuit. The ST34C86 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C86 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C86 is suitable for low power 5V operation.

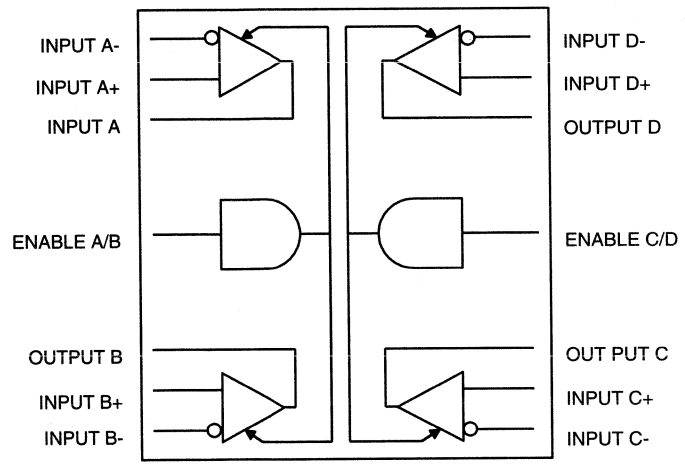
FEATURES

- Pin-to-Pin Compatible with National DS34C86
- Low Power CMOS Design
- Three-State Outputs with Enable Pin
- Meets the EIA RS-422 Requirements
- Low Propagation Delays
- High Speed

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
ST34C86CP16	16-Lead 300 Mil PDIP	0°C to +70°C
ST34C86CF16	16-Lead 150 Mil JEDEC SOIC	0°C to +70°C
ST34C86IP16	16-Lead 300 Mil PDIP	-40°C to +85°C
ST34C86IF16	16-Lead 150 Mil JEDEC SOIC	-40°C to +85°C

ST34C86 BLOCK DIAGRAM



QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

GENERAL DESCRIPTION

The ST34C87 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals, special hysteresis is built in the ST34C87 circuit.

The ST34C87 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST34C87 is suitable for low power 5V operation with high input voltage protection devices.

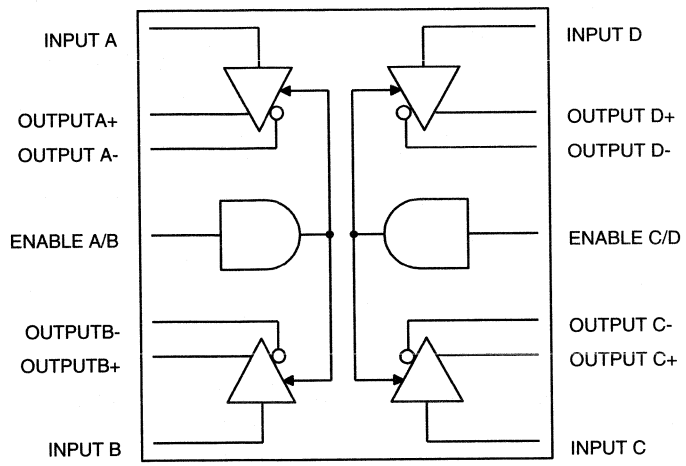
FEATURES

- Pin-to-Pin Compatible with National DS34C87
- Low Power CMOS Design
- Three-State Outputs with Enable Pin
- Meets the EIA RS-422 Requirements
- Low Propagation Delays
- High Speed

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
ST34C87CP16	16-Lead 300 Mil PDIP	0°C to +70°C
ST34C87CF16	16-Lead 150 Mil JEDEC SOIC	0°C to +70°C
ST34C87IP16	16-Lead 300 Mil PDIP	-40°C to +85°C
ST34C87IF16	16-Lead 150 Mil JEDEC SOIC	-40°C to +85°C

ST34C87 BLOCK DIAGRAM



GENERAL DESCRIPTION

XRT3590 is a single chip device which contains three V.35 receivers and transmitters. This device by itself is sufficient to implement all the data and clock signals required for a V.35 interface. For the handshaking signals, separate RS-232 transceivers are necessary.

This device supports multiple modes of operation including DCE and DTE. Diagnostic loopbacks are supported both in the DCE and DTE modes. To accommodate diagnostics in both directions, a mirrored loopback is implemented. Both clock and data paths are looped back during the diagnostics mode. This feature can be invoked by applying appropriate patterns to SEL lines. (See Table 1.) For power management flexibility, all of the drivers and receivers can be placed in a shut down mode. For applications where only receivers are required, all the drivers can be disabled and vice versa. During disable mode the output drivers are placed in Hi-Z state.

The differential V.35 output drivers of this device are implemented using a current mode type design. This minimizes the number of external resistors required. Due to low voltage swing required in the current mode of operation, the emission in a typical V.35 interface using this device is minimized. Each transmitter and receiver would require an external resistor network consisting of 3 resistors for termination. This device does not require any large capacitors in addition to two 0.1mF decoupling caps needed across the power supplies. In order to reduce the number of external components, resistor network can be used to realize both the driver and receiver termination.

FEATURES

- Single device provides three receivers and transmitters fully compliant with electrical specification of V.35 interface (receiver differential inputs are V.11 compliant)
- Supports all V.35 clock and data signals in DTE and DCE modes of operation
- Transmitters are short circuit protected
- Supports a maximum data rate of 10MBPS up to 100 meters
- Full compliance with ITU-T V.35 specification
- Supports mirrored diagnostic loop backs in DTE and DCE modes of operation
- Allows disabling all receivers, or all drivers, or all receivers and drivers
- During the disable mode the outputs are placed in Hi-Z state
- Maximum power dissipation 540mW (All active mode)
- Maximum power consumption 600mW (All drivers loaded)
- Current consumption during shut down mode is less than 300mA

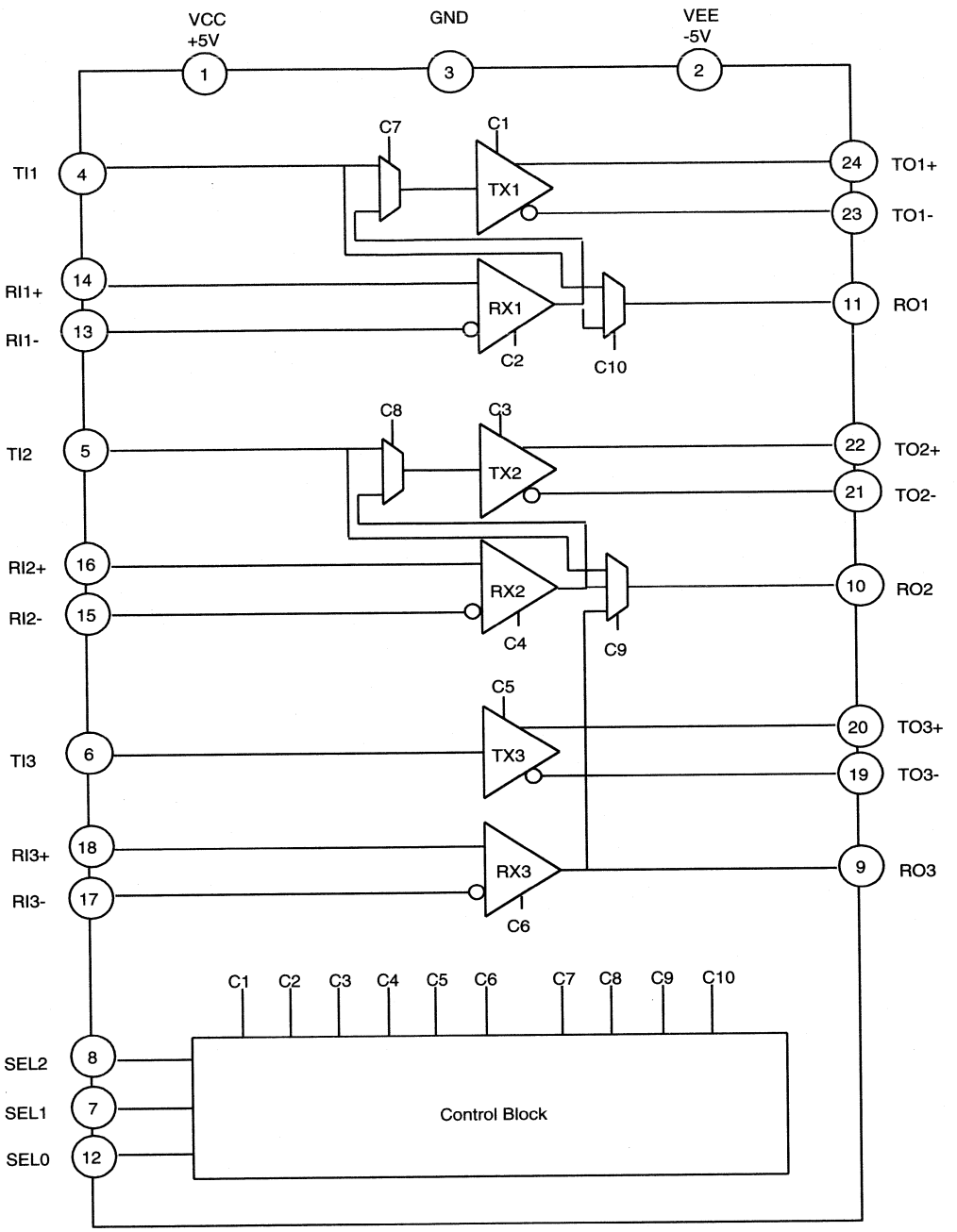
APPLICATIONS

- Bridges and Routers
- Modems
- Digital Service Units (DSUs)
- Multiplexers
- HDSL and ADSL equipment
- Inverse Multiplexers
- Workstations

ORDERING INFORMATION

Part Number	Package	Operating Temperature Range
XRT3590IP	24-Lead 600 Mil PDIP	-40°C to +85°C
XRT3590ID	24-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

XRT3590 BLOCK DIAGRAM



GENERAL DESCRIPTION

XRT3591B is a single chip device which contains three V.35 receivers and transmitters. This device by itself is sufficient to implement all the data and clock signals required for a V.35 interface. For the handshaking signals, separate RS-232 transceivers are necessary.

This device supports multiple modes of operation including DCE and DTE. Diagnostic loopbacks are supported both in the DCE and DTE modes. To accommodate diagnostics in both direction, a mirrored loopback is implemented. Both clock and data paths are looped back during the diagnostics mode. This feature can be invoked by applying appropriate patterns to SEL lines. (See Table 1.) For power management flexibility, all of the drivers and receivers can be placed in a shut down mode. For applications where only receivers are required, all the drivers can be disabled and vice versa. During disable mode the output drivers are placed in Hi-Z state.

The differential V.35 output drivers of this device are implemented using a current mode type design. This minimizes the number of external resistors required. Due to low voltage swing required in the current mode of operation, the emission in a typical V.35 interface using this device is minimized. Each transmitter and receiver would require an external resistor network consisting of 3 resistors for termination. This device does not require any large capacitors in addition to two 0.1mF decoupling caps needed across the power supplies. In order to reduce the number of external components, resistor network can be used to realize both the driver and receiver termination.

FEATURES

- Single Device Provides Three Receivers and Transmitters Fully Compliant with Electrical Specification of V.35 Interface (Receiver Differential Inputs are V.11 Compliant)
- Supports all V.35 Clock and Data Signals in DTE and DCE Modes of Operation
- Transmitters Are Short Circuit Protected
- Supports A Maximum Data Rate Of 10 MBPS Up To 100 Meters
- Full Compliance with CCITT V.35 Specification
- Supports Mirrored Diagnostic Loopbacks in DTE and DCE Modes of Operation
- Allows Disabling all Receivers, or all Drivers, or all Receivers and Drivers
- During the Disable Mode the Outputs are placed in Hi-Z State
- Maximum Power Dissipation 540mW (All Active Mode)
- Maximum Power Consumption 600mW (All Drivers Loaded)
- Current Consumption During Shut Down Mode is less than 300mA

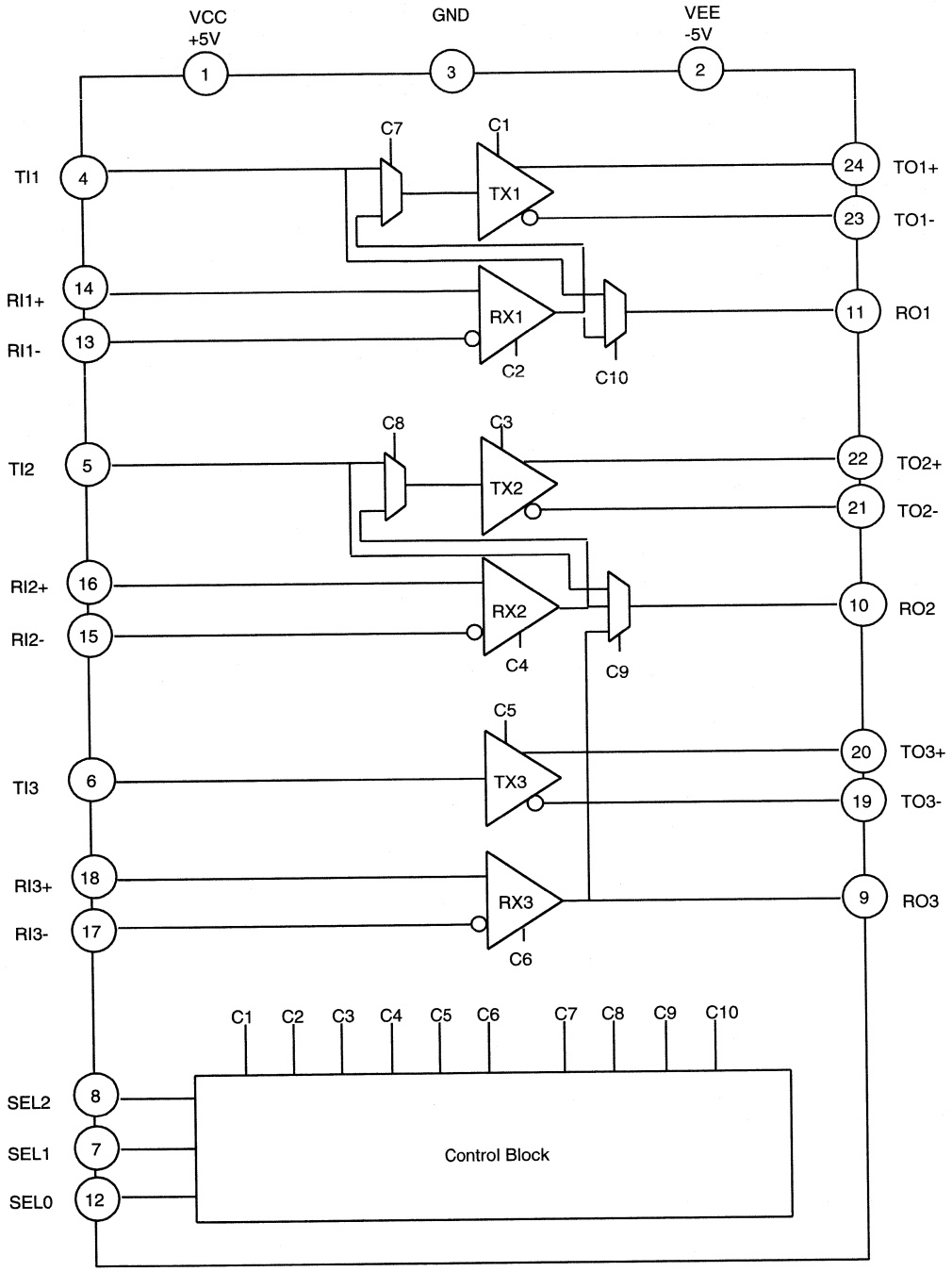
APPLICATIONS

- Bridges and Routers
- Modems
- Digital Service Units (DSUs)
- Multiplexers
- HDSL and ADSL equipment
- Inverse Multiplexers
- Workstations

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT3591BIP	24-Lead 600 Mil PDIP	-40°C to +85°C
XRT3591BID	24-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

XRT3591B BLOCK DIAGRAM



MULTIPROTOCOL SERIAL NETWORK INTERFACE

GENERAL DESCRIPTION

The XRT4500 is a fully integrated multiprotocol serial interface. It supports all of the popular serial communication interface standards such as ITU-T V.35, ITU-T V.36, EIA530A, RS232 (ITU-T V.28), ITU-T X.21 and RS449. It can easily be interfaced with most common types of Serial Communications Controllers (SCCs). This device contains eight receivers and eight transmitters, in groups of six or seven. It is a complete solution containing all of the required source and load termination resistors in one 80-pin TQFP package. The XRT4500 operates at higher speeds (20MHz for V.35 and 256kbps for V.28).

The XRT4500 can be configured to operate in one of the seven interface standards in either DTE, or DCE modes of operation and power down mode. It fully supports echoed clock as well as clock and data inversion. Loopbacks are supported in DTE and DCE modes of operation. This feature eliminates the need for external circuitry for loopback implementation. Control signals such as RI, RL, DCD, DTR, DSR are protected against glitches by internal filters. These filters can be turned off. The XRT4500 provides an internal oscillator (clock signal) which can be used to conduct standalone diagnostics of DTE equipment.

FEATURES

- Pin Programmable Multiprotocol Serial Interface
- V.35, V.36, EIA-530 A, RS232 (V.28), V.10, V.11, X.21 and RS449 Communication Interface Standards
- V.28, V.10, V.11 and V.35 Electrical Interfaces are 'CTR2' Compliant
- Contains On-Chip Source and Load Termination Resistors
- Contains Eight Receivers and Eight Transmitters with Switchable DTE and DCE Modes
- Glitch Filters on the Control Signals (Selectable)
- +5V Single Power Supply with internal DC-DC Converter
- Full Support of Loopbacks, Data & Clock Inversion, and Echoed Clock in DTE and DCE Modes
- Full Support of Most Popular Types of HDLC Controllers (Single, Double, and Triple Clocks supported)
- High-speed V.28 Driver: 256KHz
- Internal Oscillator for Standalone DTE Loopback Testing
- Control Signals Can Be Registered and Non-registered
- Control Signals Can Be Tri-stated for Bus-based Designs
- "Cable Safe" Operation Supported
- ESD Protection Over ± 1KV Range
- TTL Level Digital Inputs
- TTL/CMOS Digital Outputs

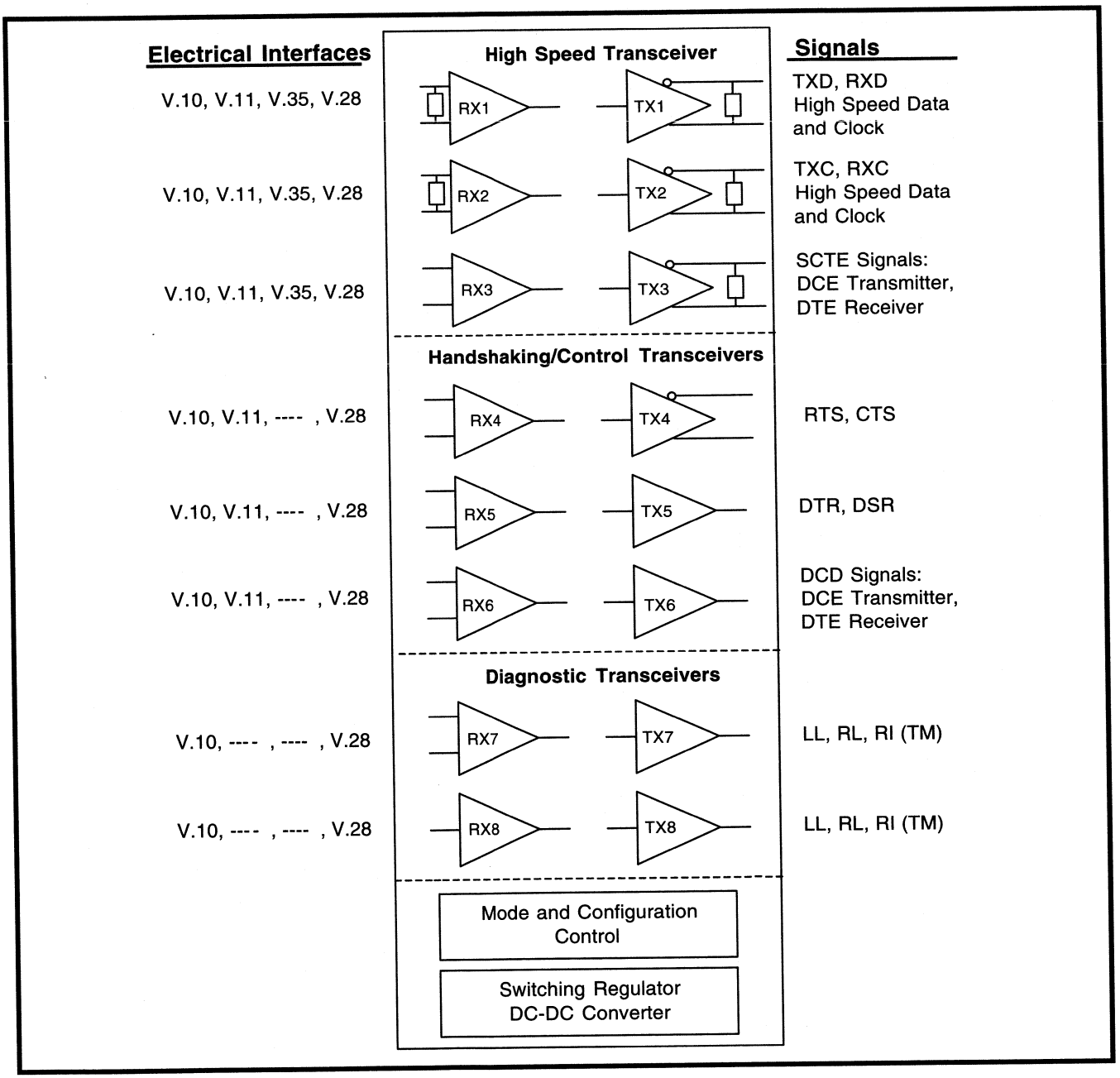
APPLICATIONS

- Data Service Units (DSU)
- Channel Service Units (CSU)
- Routers
- Bridges
- Access Equipment

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT4500CV	80-Lead TQFP	0°C to +70°C

XRT4500 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT5683A is a PCM line interface chip consisting of both transmit and receive circuitry. This device is offered in a plastic dual in-line (PDIP) or in a surface mount package (SOIC). The maximum bit rate of the chip is 8.448Mbps, and the signal level to the receiver can be attenuated by -10dB cable loss at one-half the bit rate. At nominal supply voltage operation, the typical current consumption is 40mA.

FEATURES

- Single 5V Supply
- Receiver Input Can Be Either Balanced or Unbalanced
- Up To 8.448Mbps Operation In Both Tx and Rx Directions
- TTL Compatible Interface
- Device Can Be Used as a Line Interface Unit Without Clock Recovery

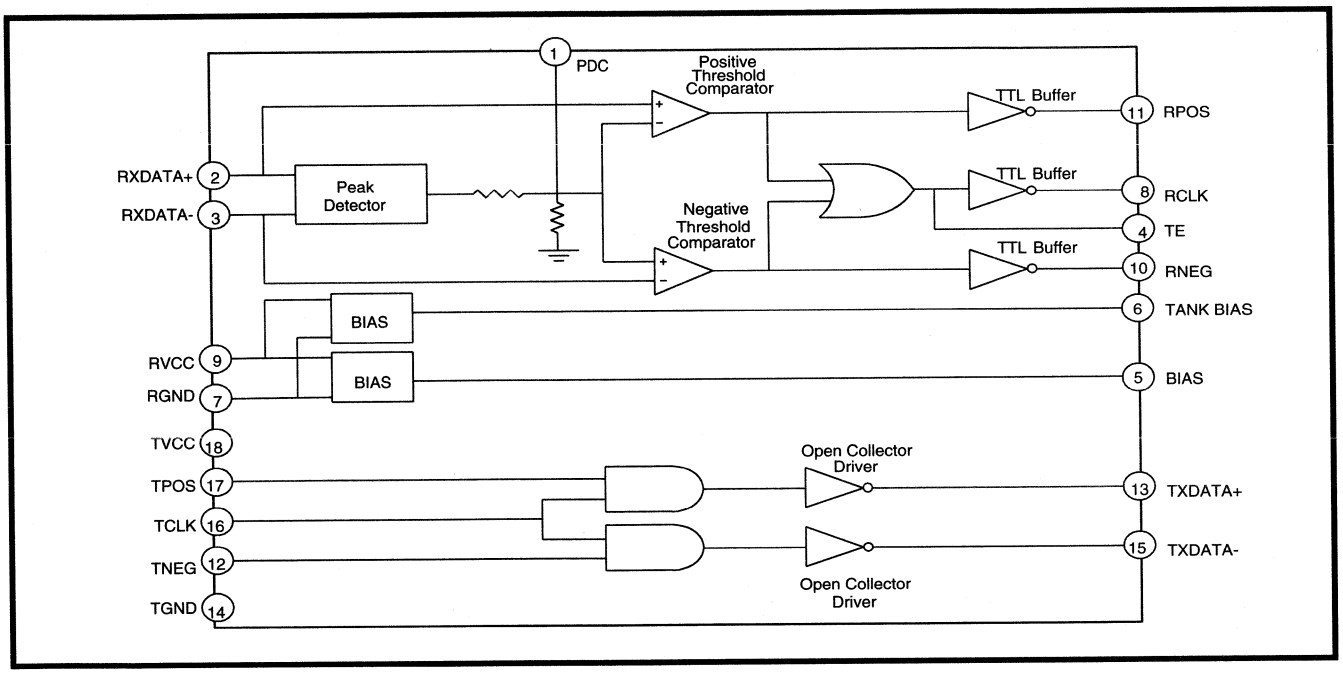
APPLICATIONS

- T1, T2, E1 & E2 Rates, PCM Line Interface
- Network Multiplexing and Terminating Equipment

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT5683AIP	18-Lead 300 Mil PDIP	-40°C to +85°C
XRT5683AID	18-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

XRT5893A BLOCK DIAGRAM



FOUR-CHANNEL E1 LINE INTERFACE (3.3V OR 5.0V)

GENERAL DESCRIPTION

The XRT5894 is an optimized four channel 3.3V line interface unit fabricated using low power CMOS technology. The device contains four independent E1 channels. Each channel performs the driver and receiver functions necessary to convert bipolar signals to logical levels and vice versa. The device requires transformers on both receiver and transmitter sides, and supports both balanced and unbalanced interfaces.

The device offers two distinct modes of LOS detection. The first method, which does not require an external clock, provides an LOS output indication signal with thresholds and delay that comply with the ITU G.775 requirements. In the second mode, the user provides an external clock that increases the delay for LOS declaration and clearing. This feature provides the user with the flexibility to implement LOS specifications that require a delay greater than the G.775 requirements.

FEATURES

- Compliant with ITU G.703 Pulse Mask Template for 2.048Mbps (E1) Rates
- Four Independent CEPT Transceivers
- Supports Differential Transformer Coupled
- Receivers and Transmitters
- On Chip Pulse Shaping for Both 75W and 120W Line Drivers
- Compliant with ITU G.775 LOS Declaration/Clearing Recommendation
- Optional User Selectable LOS Declaration/Clearing Delay
- Logical Inputs Accept either 3.3V or 5.0V Levels
- Ultra-Low Power Dissipation
- +3.3V or 5.0V Supply Operations
- Individual Transmit Channel Over Temperature Protection

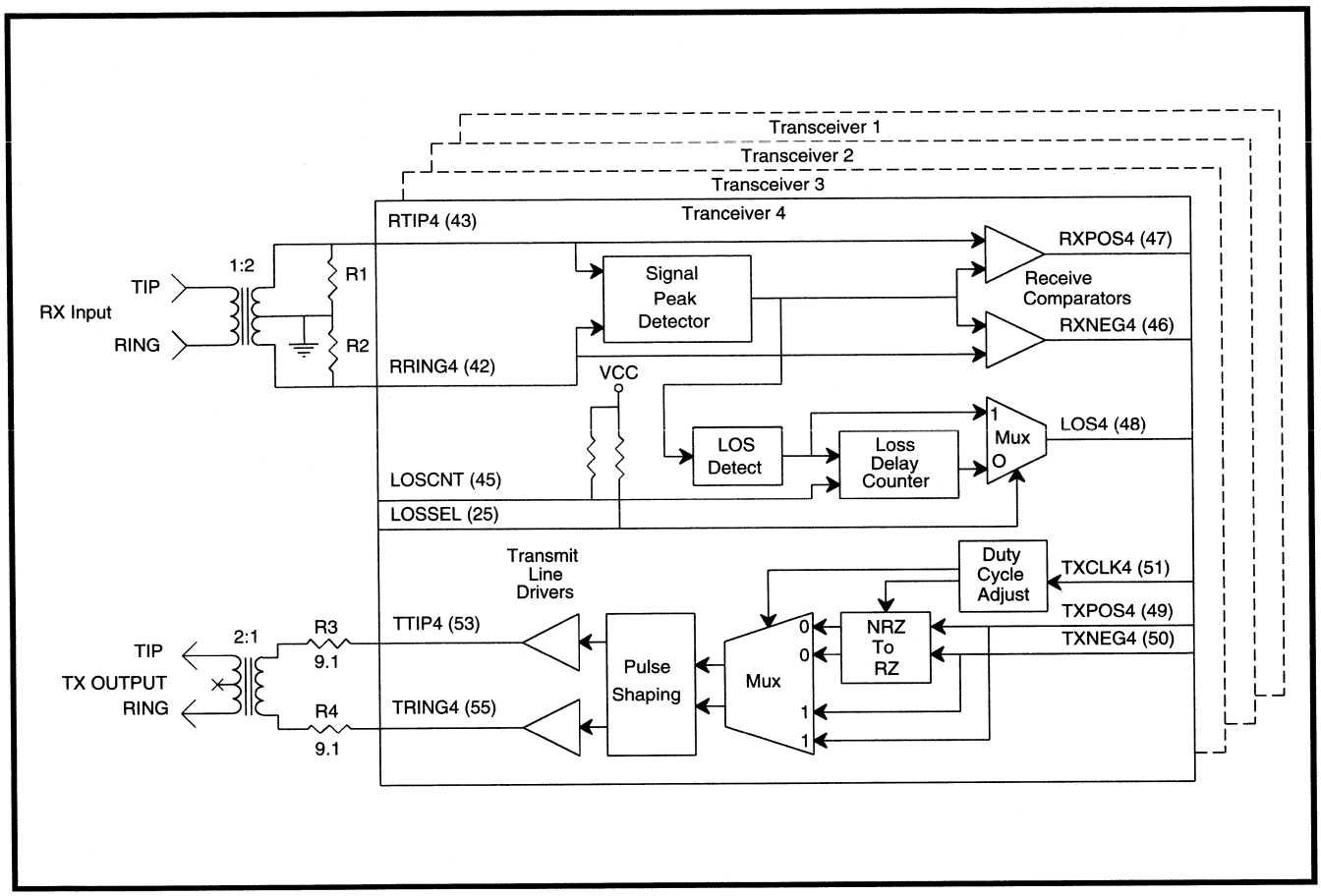
APPLICATIONS

- SDH Multiplexer
- Digital Cross Connects

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT5894IV	64-Lead TQFP (10 x 10 x 1.4mm)	-40°C to +85°C

XRT5894 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT5897 is an optimized seven channel 3.3V line interface unit fabricated using low power CMOS technology. The device contains seven independent E1 channels. It is primarily targeted toward SDH multiplexers that accommodate TU12 Tributary Unit Frames. Line cards in these units multiplex 21 E1 interfaces into higher SDH rates. Devices with seven E1 interfaces such as the XRT5897 provide the most efficient method of implementing 21 channel line cards. Each channel performs the driver and receiver functions necessary to convert bipolar signals to logical levels and vice versa. The device requires transformers on both receiver and transmitter sides, and supports both balanced and unbalanced interfaces.

The device offers two distinct modes of LOS detection. The first method, which does not require an external clock, provides an LOS output indication signal with thresholds and delay that comply with the ITU G.775 requirements. In the second mode, the user provides an external clock that increases the delay for LOS declaration and clearing. This feature provides the user with the flexibility to implement LOS specifications that require a delay greater than the G.775 requirements.

FEATURES

- Compliant with ITU G.703 Pulse Mask Template for 2.048Mbps (E1) Rates
- Seven Independent CEPT Transceivers
- Supports Differential Transformer Coupled Receivers and Transmitters
- On Chip Pulse Shaping for Both 75W and 120W Line Drivers
- Compliant with ITU G.775 LOS Declaration/Clearing Recommendation
- Optional User Selectable LOS Declaration/Clearing Delay
- Logical Inputs Accept either 3.3V or 5.0V Levels
- Ultra-Low Power Dissipation
- +3.3V Supply Operation
- Individual Transmit Channel Over Temperature Protection

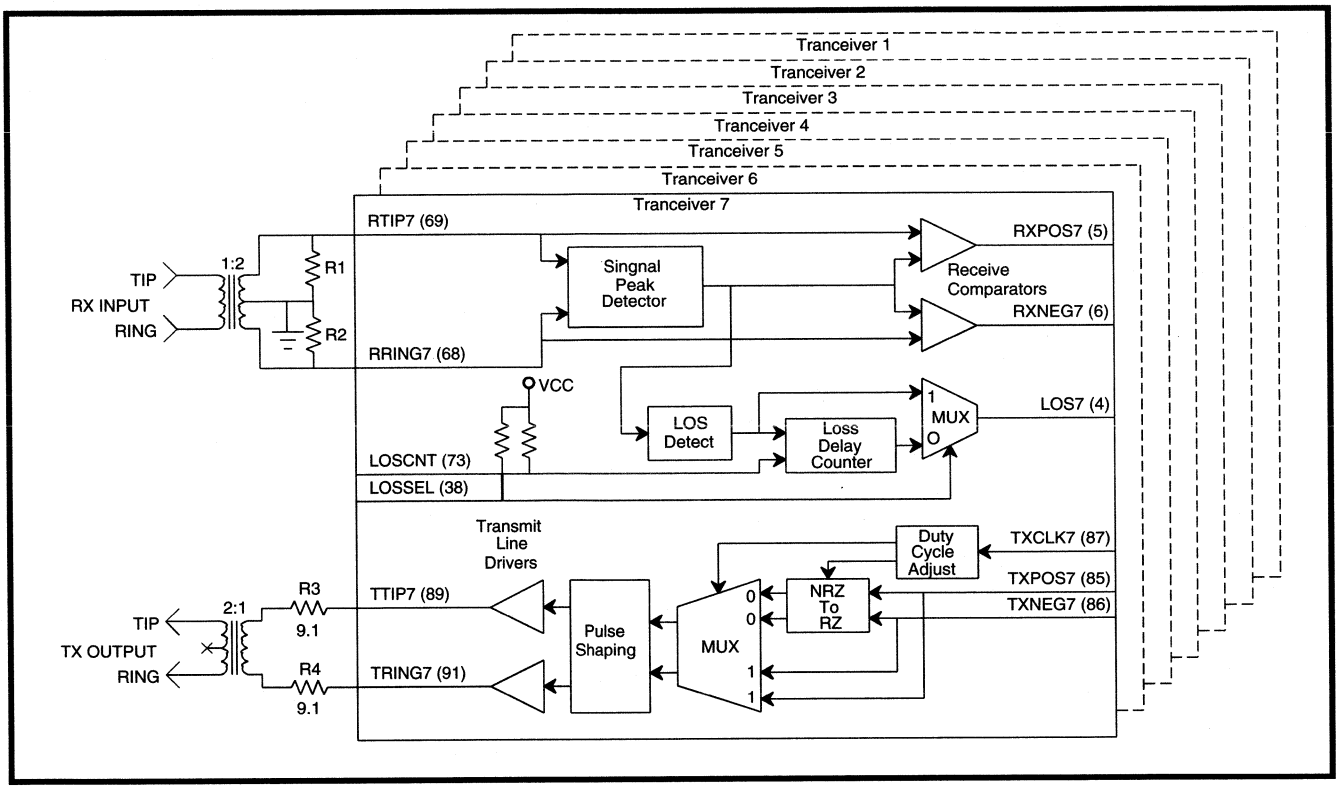
APPLICATIONS

- SDH Multiplexer
- Digital Cross Connects

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT5897IV	100-Lead TQFP (14 x 14 x 1.4mm)	-40°C to +85°C

XRT5897 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT59L91 is an optimized single-chip analog 3.3V E1 line interface unit (LIU) fabricated using low power CMOS technology. The LIU IC consists of both a Transmitter and a Receiver function. The Transmitter accepts a TTL or CMOS level signal from the Terminal Equipment; and outputs this data to the line via bipolar pulses that are compliant to the ITU-T G.703 pulse template for E1. The Receiver accepts an attenuated bipolar line signal (from the remote terminal equipment) and outputs this data to the (near-end) terminal equipment via CMOS level signals.

The receiver input can be transformer- or capacitively-coupled to the line. If the receiver input is transformer-coupled to the line, then it should be so, via the 2:1 step-down transformer. The transmitter is coupled to the line using a 1:2 step-up transformer. This same configuration is applicable for both balanced (120Ω) and unbalanced (75Ω) interfaces.

FEATURES

- Complete E1 (CEPT) line interface unit (Transmitter and Receiver)
- Generates transmit output pulses that are compliant with the ITU-T G.703 Pulse Template for 2.048Mbps (E1) rates
- On-Chip Pulse Shaping for both 75Ω and 120Ω Line Drivers
- Receiver can either be transformer or capacitively-coupled to the line
- Detects and Clears LOS (Loss of Signal) per ITU-T G.775
- Compliant with the ITU-T G.823 Jitter Tolerance Requirements
- Compliant with the ITU-T G.703 EOS Over-voltage protection requirements
- Supports both Local- and Remote-Loop back Operations
- Logic Inputs accept either 3.3V or 5.0V levels
- Operates over the Industrial Temperature Range
- Ultra Low Power Dissipation
- +3.3V Supply Operation

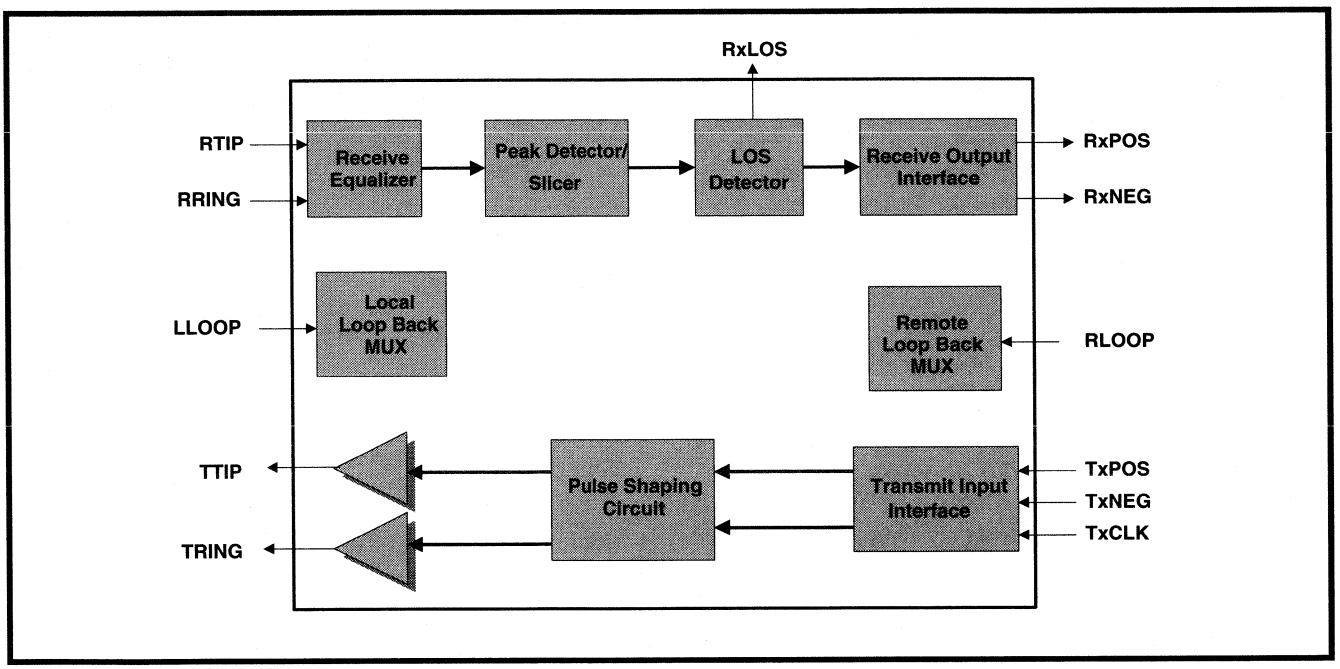
APPLICATIONS

- PDH Multiplexers
- SDH Multiplexers
- Digital Cross-Connect Systems
- DECT (Digital European Cordless Telephone) Base Stations
- CSU/DSU Equipment.
- Test Equipment

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT59L91ID	16-Lead JEDEC SOIC (300 mil)	-40°C to +85°C

XRT59L91 BLOCK DIAGRAM



SEVEN-CHANNEL E1 LINE INTERFACE UNIT

GENERAL DESCRIPTION

The XRT5997 is an optimized seven-channel analog 3.3V E1 line interface unit fabricated using low power CMOS technology. Each LIU channel consists of both a Transmitter and a Receiver function. The Transmitter accepts a TTL or CMOS level signal from the Terminal Equipment; and outputs this data to the line via bipolar pulses that are compliant to the ITU-T G.703 pulse template for E1. The Receiver accepts an attenuated bipolar line signal (from the remote terminal equipment) and outputs this data to the (near-end) terminal equipment via CMOS level signals.

Each Receiver input can be transformer- or capacitive-coupled to the line. If the Receiver input is transformer-coupled to the line, then it should be so, via a 2:1 step-down transformer. Each Transmitter is coupled to the line using a 1:2 step-up transformer. This same configuration is applicable for both balanced (120Ω) and unbalanced (75Ω) interfaces.

FEATURES

- Consists of Seven (7) Independent E1 (CEPT) Line Interface Units (Transmitter and Receiver)

PER CHANNEL FEATURES

- Generates Transmit Output Pulses that are Compliant with the ITU-T G.703 Pulse Template Requirement for 2.048Mbps (E1) Rates
- On-Chip Pulse Shaping for Both 75Ω and 120Ω Line Drivers
- Receiver Can Either Be Transformed or Capacitive-Coupled to the Line
- Detects and Clears LOS (Loss of Signal) Per ITU-T G.775
- Compliant with the ITU-T G.823 Jitter Tolerance Requirements
- Compliant with ITU G. 703 EOS Over-voltage protection Requirement
- Logic Inputs Accept Either 3.3V or 5.0V Levels
- Operates over the Industrial Temperature Range
- Ultra Low Power Dissipation
- +3.3V Supply Operation

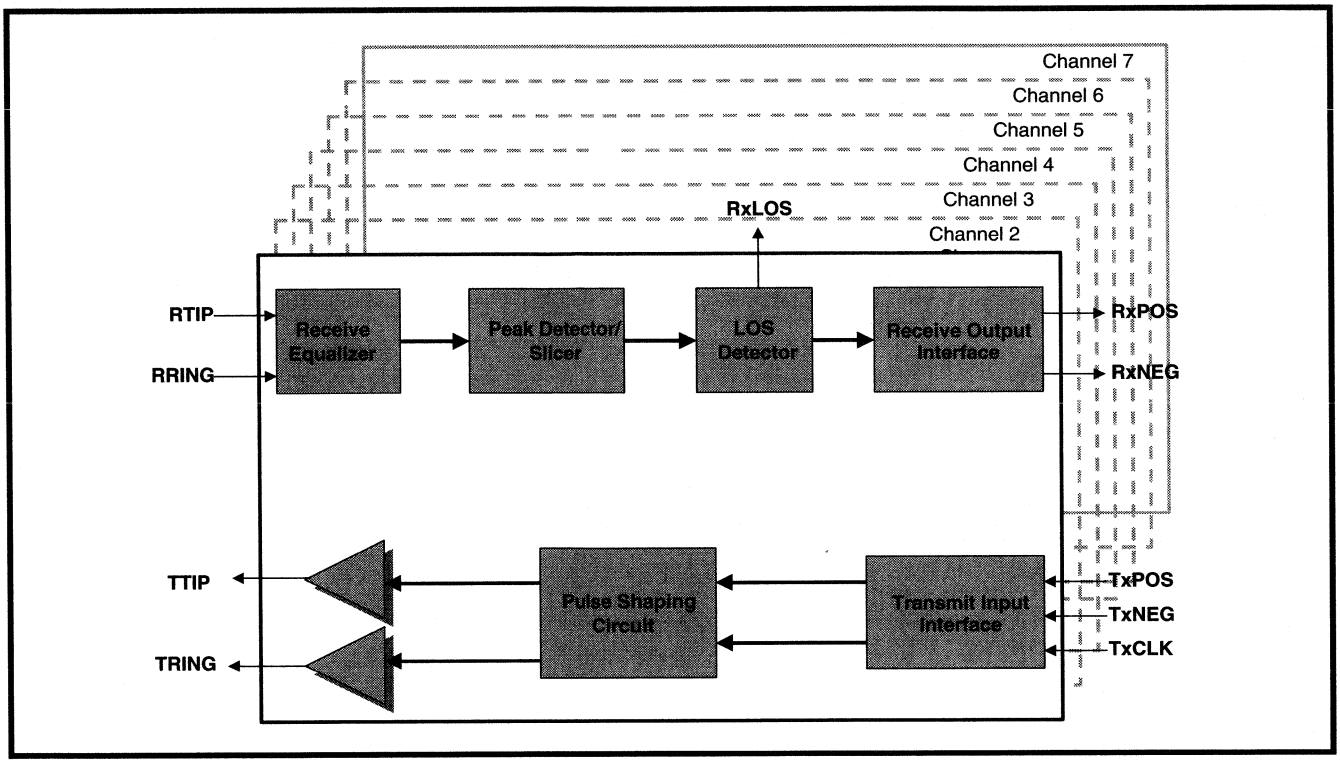
APPLICATIONS

- PDH Multiplexers
- SDH Multiplexers
- Digital Cross-Connect Systems
- DECT (Digital European Cordless Telephone) Base Stations

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT5997IV	100-Lead TQFP (14 x 14 x 1.4 mm)	-40°C to +85°C

XRT5997 BLOCK DIAGRAM



DIGITAL LINE INTERFACE TRANSCEIVER

REV. 2.02

GENERAL DESCRIPTION

The XR-T6164 is a bipolar analog chip intended for general purpose line interface applications at bit rates up to 1.544Mbps (T1). It contains both receive and transmit circuitry in a 16 pin dual-in-line plastic package. The receiver is designed for short line applications having a cable loss up to 10dB measured at the half bit rate. The transmitter has open collector line driver outputs that are capable of handling up to 40mA.

When used in conjunction with either XR-T6165 or XR-T6166, the chip set provides a 64Kbps codirectional interface as specified in CCITT G.703.

FEATURES

- Single 5V Supply
- CCITT G.703 Compatible When Used With Either XR-T6165 or XR-T6166
- Low Power
- TTL Compatible Digital Inputs and Outputs
- Links Remote Equipment at Distances up to 500 Meters Without Equalization
- Receive Data Comparator Threshold Storage
- Provides Ping-Pong Operation Capability
- Loss of Signal Alarm
- Dual Matched Driver Outputs

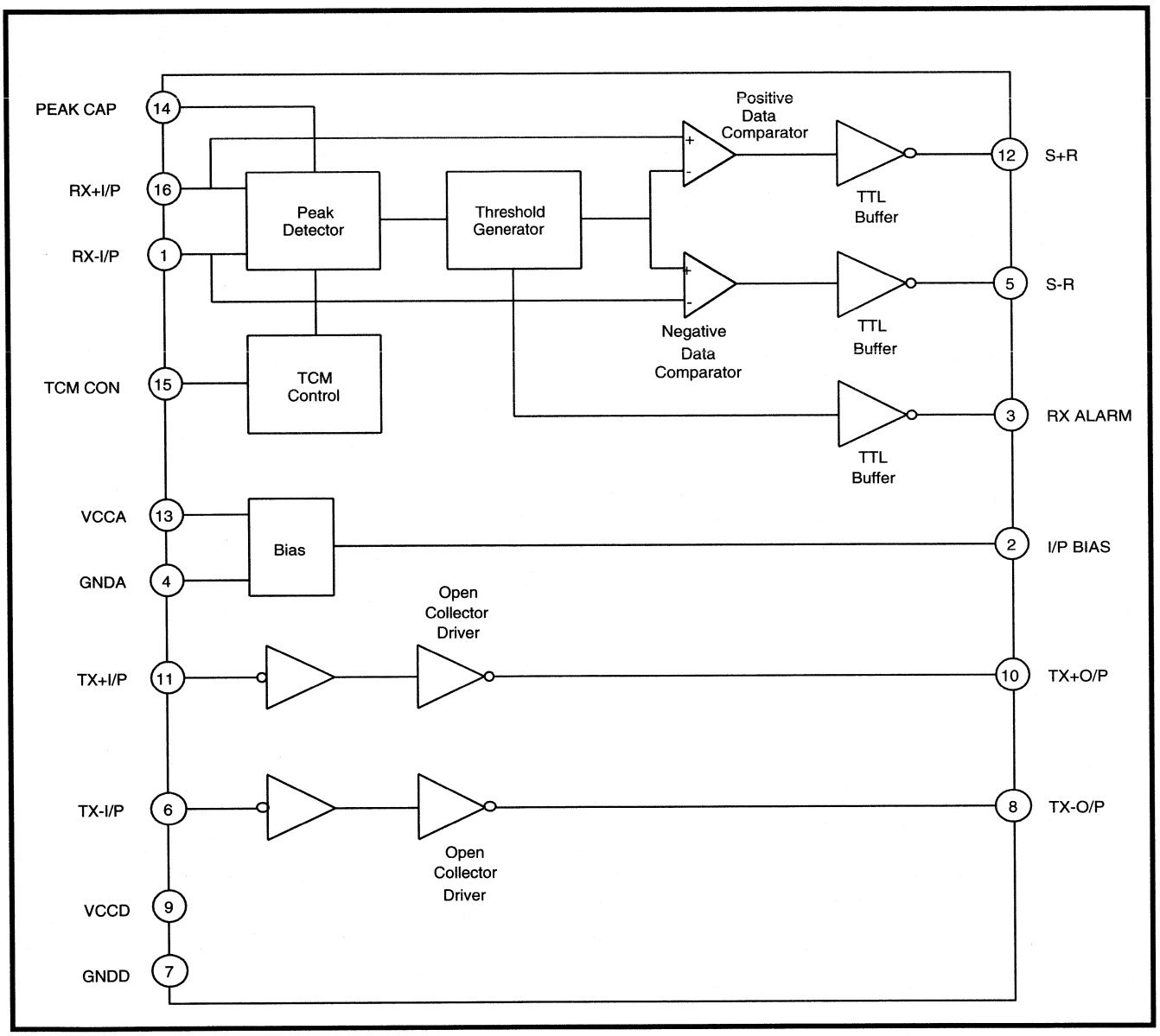
APPLICATIONS

- Data Adaption Unit (DAU)
- General Purpose TTL Compatible Line Interface

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT6164CP	16-Lead 300 Mil PDIP	0°C to +70°C
XRT6164CD	16-Lead 300 Mil JEDEC SOIC	0°C to +70°C

XRT6164 BLOCK DIAGRAM



DIGITAL LINE INTERFACE TRANSCEIVER

REV. 1.01

GENERAL DESCRIPTION

The XRT6164A is a bipolar analog chip intended for general purpose line interface applications at bit rates up to 1.544Mbps (T1). It contains both receive and transmit circuitry in a 16 pin dual-in-line plastic package. The receiver is designed for short line applications having a cable loss up to 10dB measured at the half bit rate. The transmitter has open collector line driver outputs that are capable of handling up to 40mA.

When used in conjunction with either XRT6165 or XRT6166, the chip set provides a 64Kbps codirectional interface as specified in CCITT G.703.

FEATURES

- Single 5V Supply
- Compatible with CCITT G.703 64Kbps Co-Directional Interface Recommendation When Used With Either XRT6165 or XRT6166
- Low Power
- Converts Balanced Bipolar Transmit and Receive Signals Propagated Over Two Twisted Pair Cables to TTL Compatible Dual-Rail Data
- Links Remote Equipment Equipped With CCITT G.703 64Kbps Co-Directional Interfaces Over DIstances Up to 500 Meters Without Equlaization
- Receive Data Comparator Threshold Storage
- Provides Ping-Pong Operation Capability
- Loss of Signal Alarm
- Dual Matched Driver Outputs

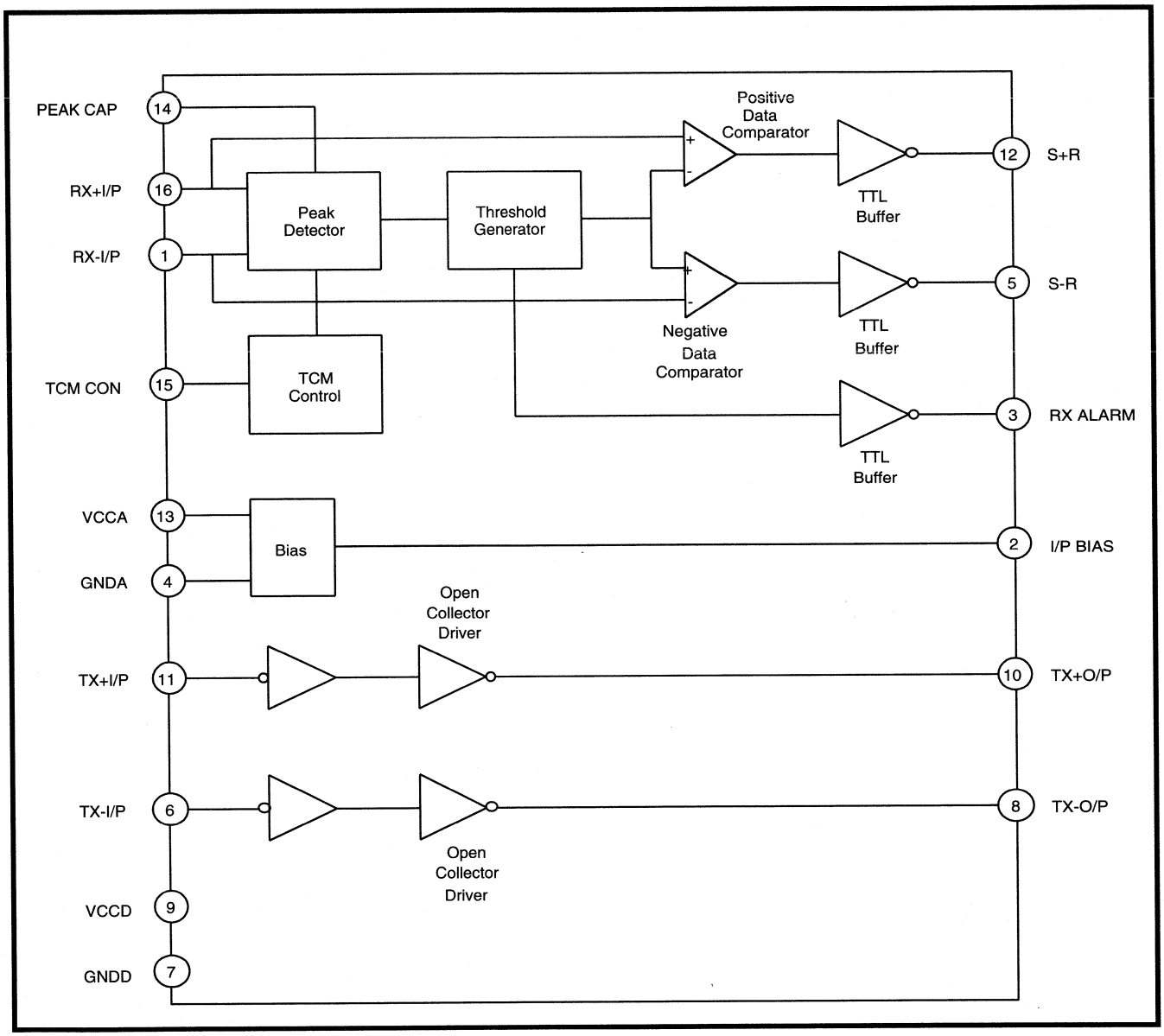
APPLICATIONS

- Data Adaption Unit (DAU)
- General Purpose TTL Compatible Line Interface

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT6164AIP	16-Lead 300 Mil PDIP	-10°C to +85°C
XRT6164AID	16-Lead 300 Mil JEDEC SOIC	-10°C to +85°C

XRT6164A BLOCK DIAGRAM



CODIRECTIONAL DIGITAL DATA PROCESSOR

GENERAL DESCRIPTION

The XRT6165 is a CMOS device which contains the digital circuitry necessary to interface both directions of a 64kbps data stream to 2.048Mbps transmit and receive PCM time-slots. The XRT6165 and the companion XRT6164 line interface chip together form a CCITT G.703 compliant 64kbps codirectional interface.

The XR-T6165 contains separate transmit and receive sections. The transmitter transforms 8 bit serial data from a 2.048Mbps time-slot into an encoded 64kbps data stream. The receiver, which performs the reverse operation, decodes the 64kbps data, extracts a clock signal, and then outputs the data to a 2.048Mbps time-slot. The XRT6165 provides features which allow the repetitions and deletions of both received and transmitted data as clock skews and transients occur.

FEATURES

- Low Power CMOS Technology
- All Receiver and Transmitter Inputs and Outputs are TTL Compatible
- Transmitter Inhibits Bipolar Violation Insertion for Transmission of Alarm Conditions
- Alarm Output Indicates Loss of Received Bipolar
- Violations
- Up to 125ms Variance of Data Transfer Timing in Both Transmit and Receive Paths Allows Operation in Plesiochronous Networks
- Both Receiver and Transmitter Perform Byte
- Insertion or Deletion in Response to Local Clock Slips

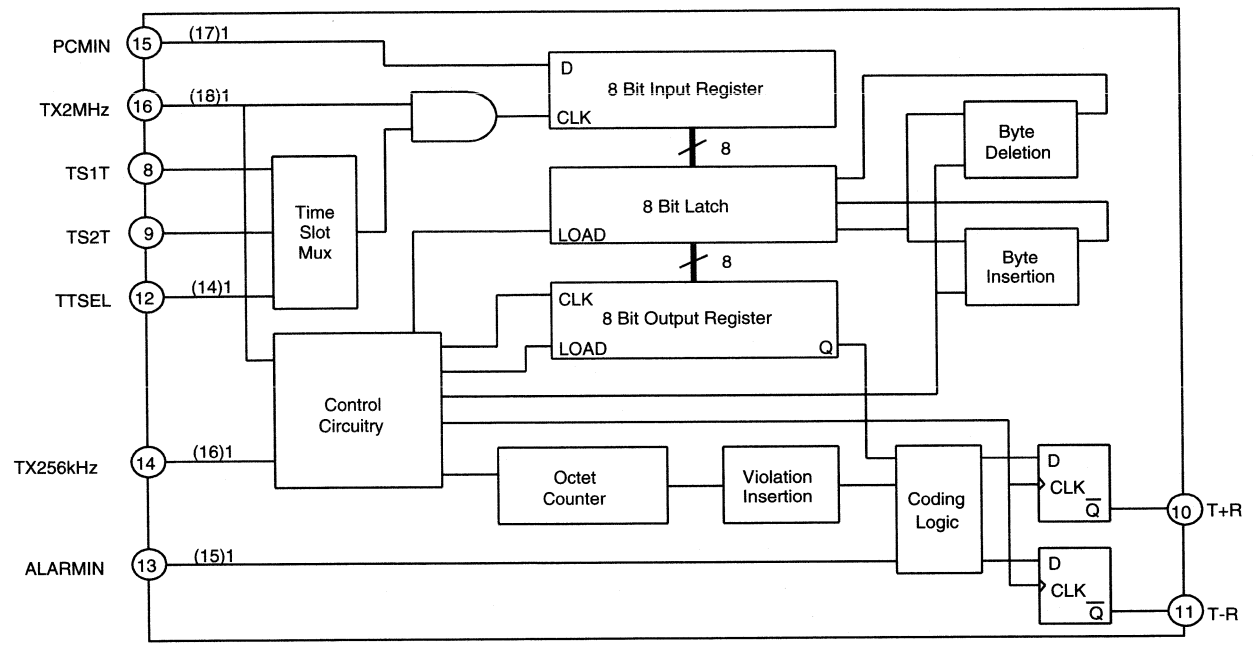
APPLICATIONS

- CCITT G.703 Compliant 64kbps Codirectional Interface
- Performs the Digital and Analog Functions for a Complete 64kbps Data Adaption Unit (DAU) When Used With the XRT6164

ORDERING INFORMATION

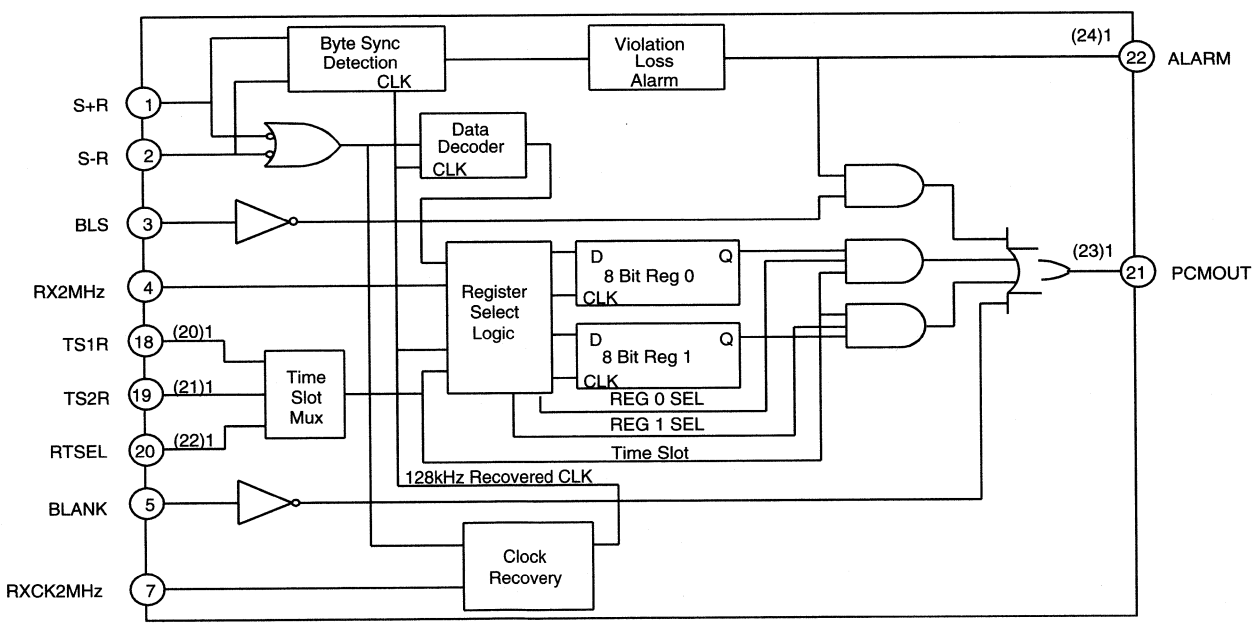
PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT6165CP	22-Lead 400 Mil PDIP	0°C to +70°C
XRT6165IP	22-Lead 400 Mil PDIP	-40°C to +85°C
XRT6165CD	24-Lead 300 Mil JEDEC SOIC	0°C to +70°C
XRT6165ID	24-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

BLOCK DIAGRAM



Note:
[1] Number in brackets are for SOIC package

XRT6165 Transmit Section Block Diagram



Note:
[1] Number in brackets are for SOIC package

XRT6165 Receiver Section Block Diagram

CODIRECTIONAL DIGITAL DATA PROCESSOR

REV. 2.02

GENERAL DESCRIPTION

The XRT6166 is a CMOS device which contains the digital circuitry necessary to interface both directions of a 64kbps data stream to 2.048Mbps transmit and receive PCM time-slots. The XRT6166 and the companion XR-T6164 line interface chip together form a CCITT G.703 compliant 64kbps codirectional interface.

The XRT6166 contains separate transmit and receive sections. The transmitter transforms 8 bit serial data from a 2.048Mbps time-slot into an encoded 64kbps data stream. The receiver, which performs the reverse operation, decodes the 64kbps data, extracts a clock signal, and then outputs the data to a 2.048Mbps time-slot. The XRT6166 provides features which allow the repetitions and deletions of both received and transmitted data as clock skews and transients occur. These slip occurrences are indicated by byte insertion and deletion flags. Outputs are also provided for extracted receive clock and clock recovery circuit loss of lock.

FEATURES

- Low Power CMOS Technology
- All Receiver and Transmitter Inputs and Outputs are TTL Compatible
- Transmitter Inhibits Bipolar Violation Insertion for Transmission of Alarm Conditions
- Alarm Output Indicates Loss of Received Bipolar Violations
- Tolerance of 125ms Variance of Data Transfer
- Timing in Both Transmit and Receive Paths
- Allows Operation in Plesiochronous Networks
- Both Receiver and Transmitter Perform Byte
- Insertion or Deletion in Response to Local Clock Slips and Provide Outputs Indicating Slip Logic Activity

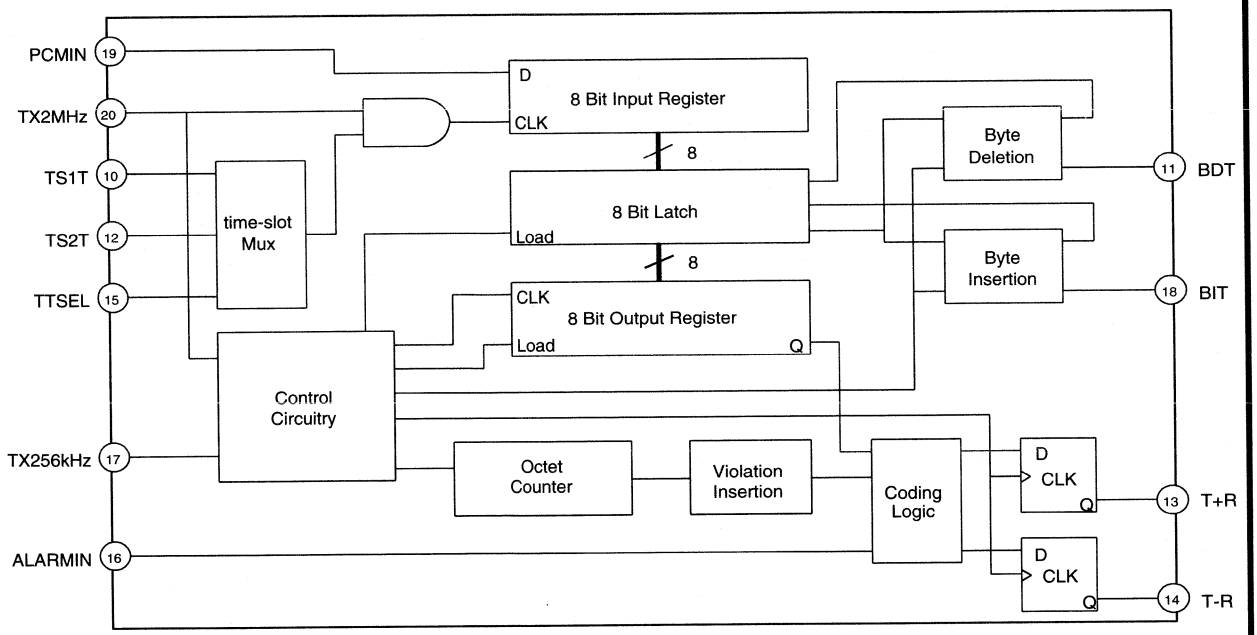
APPLICATIONS

- CCITT G.703 Compliant 64kbps Codirectional Interface
- Performs the Digital and Analog Functions for a Complete 64kbps Data Adaption Unit (DAU) When Used With the XRT6164

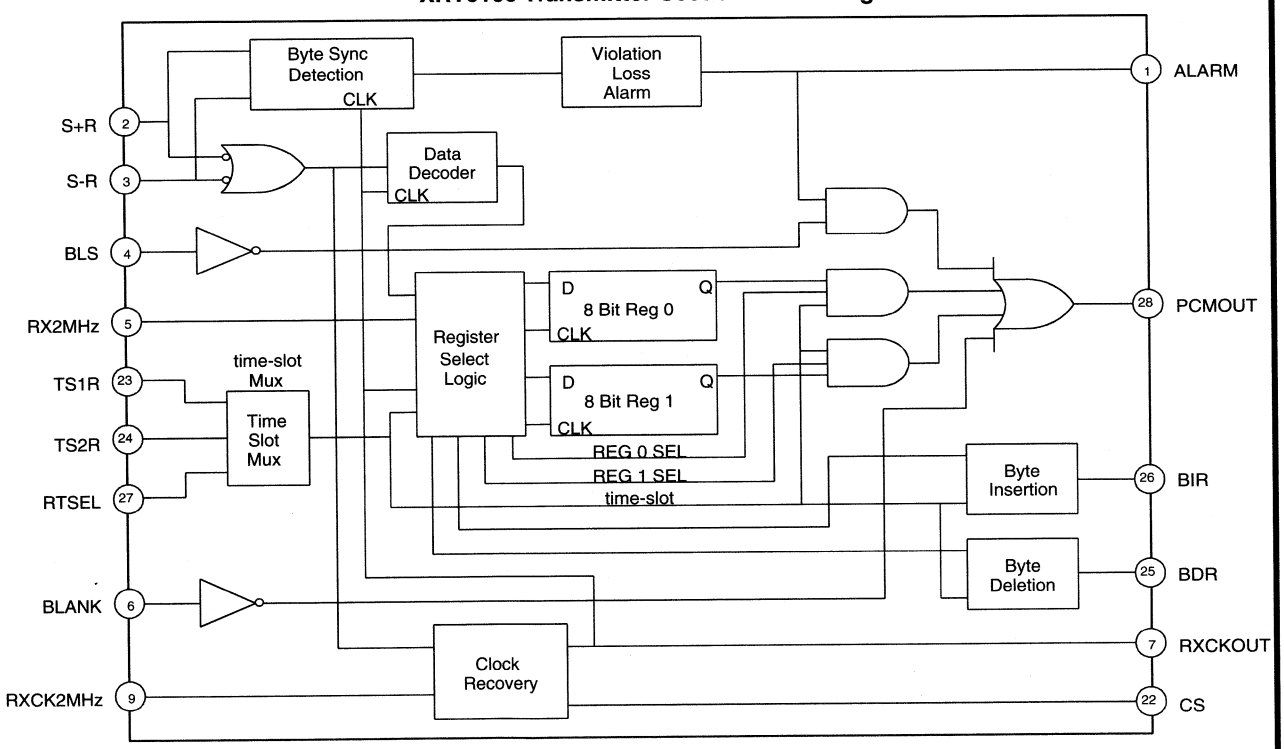
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT6166CP	28-Lead 600 Mil PDIP	0°C to +70°C
XRT6166IP	28-Lead 600 Mil PDIP	-40°C to +85°C
XRT6166CD	28-Lead 300 Mil JEDEC SOIC	0°C to +70°C
XRT6166ID	28-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

XRT6166 BLOCK DIAGRAM



XRT6166 Transmitter Section Block Diagram



XRT6166 Receiver Section Block Diagram

DS3/E3/STS-1 JITTER ATTENUATOR, STS-1 TO DS3 DESYNCHRONIZER

REV. 1.01

GENERAL DESCRIPTION

The XRT71D00 is a single channel, single chip Jitter Attenuator, that meets the Jitter requirements specified in the ETSI TBR-24, Bellcore GR-499 and GR-253 standards.

In addition, the XRT71D00 also meets the Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253 and GR-499 standards for Desynchronizing and Pointer adjustments in the DS3 to STS-SPE mapping applications.

FEATURES

- Meets the E3/DS3/STS-1 jitter requirements
- No external components required
- Compliance with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Meets output jitter requirement as specified by ETSI TBR24
- Meets the Jitter and Wander specifications described in T1.105.03b,GR-253 and GR-499 standards.
- Selectable buffer size of 16 and 32 bits
- Jitter attenuator can be disabled
- Available in a 32 pin TQFP package.
- Single 3.3V or 5.0V supply.
- Operates over - 40^0 C to 85^0 C temperature range.

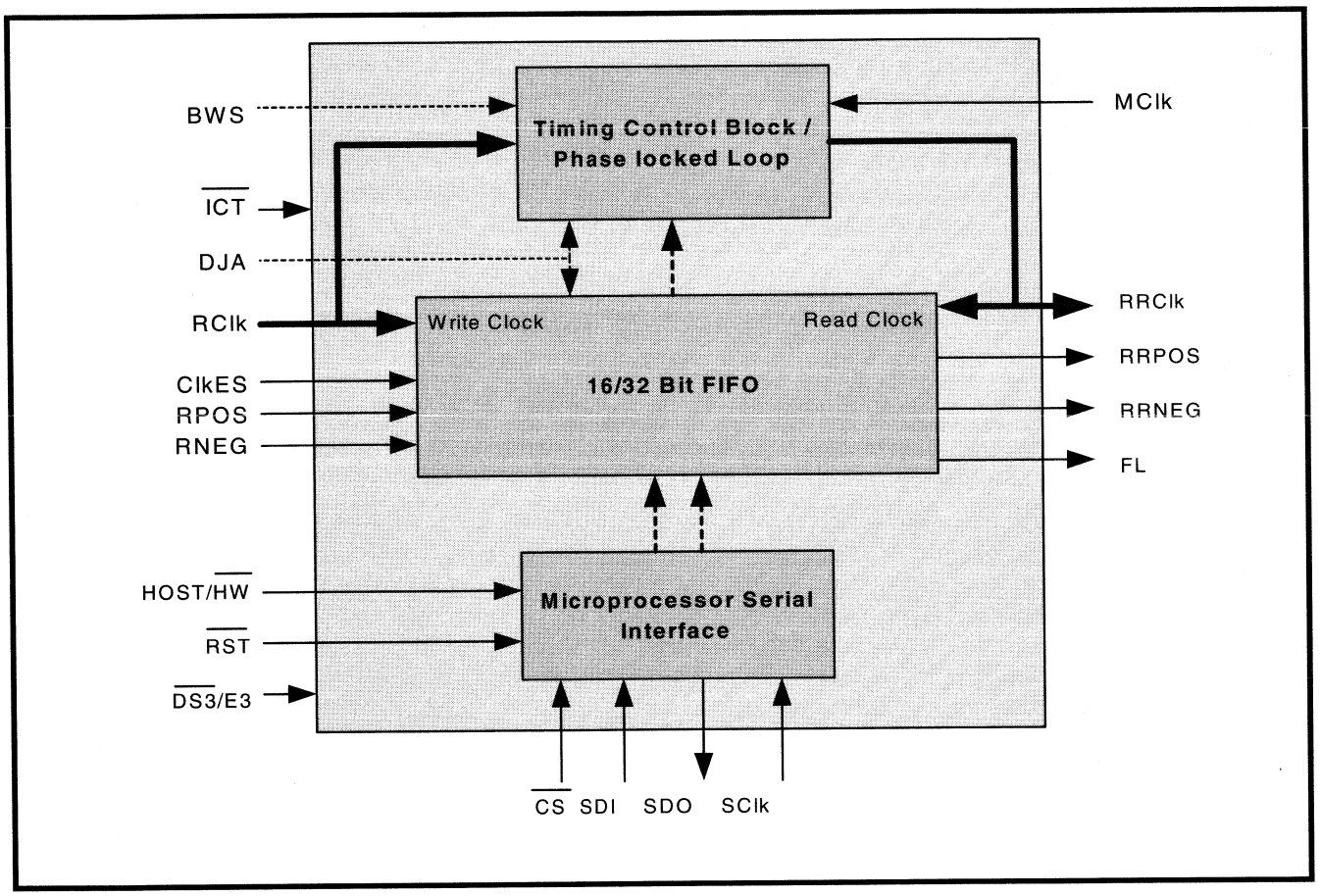
APPLICATIONS

- E3/DS3 Access Equipment.
- STS-SPE to DS3 Mapper
- DSLAMs

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D00IQ	32-Lead TQFP	-40°C to +85°C

XRT71D00 BLOCK DIAGRAM



THREE-CHANNEL DS3/E3/STS-1 JITTER ATTENUATOR, STS-1 TO DS3 DESYNCHRONIZER

REV. 1.1.1

GENERAL DESCRIPTION

The XRT71D03 is a three channel, single chip Jitter Attenuator, that meets the Jitter transfer characteristics requirements specified in the ETSI TBR-24, Bellcore GR-499 and GR-253 standards.

In addition, the XRT71D03 also meets the Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253 and GR-499 standards for Desynchronizing and Pointer adjustments in the DS3 to STS-SPE mapping applications.

FEATURES

- Meets the E3/DS3/STS-1 jitter requirements
- No external components required
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755, GR-235-CORE, GR-499-CORE,1995 standards
- Meets output jitter requirement as specified by ETSI TBR24
- Meets the Jitter and Wander specifications described in T1.105.03b,GR-253 and GR-499 standards.
- Selectable buffer size of 16 and 32 bits
- Jitter attenuator can be disabled
- Available in a 64-pin TQFP package.
- Single 3.3V or 5.0V supply.
- Operates over - 40° C to 85° C temperature range.

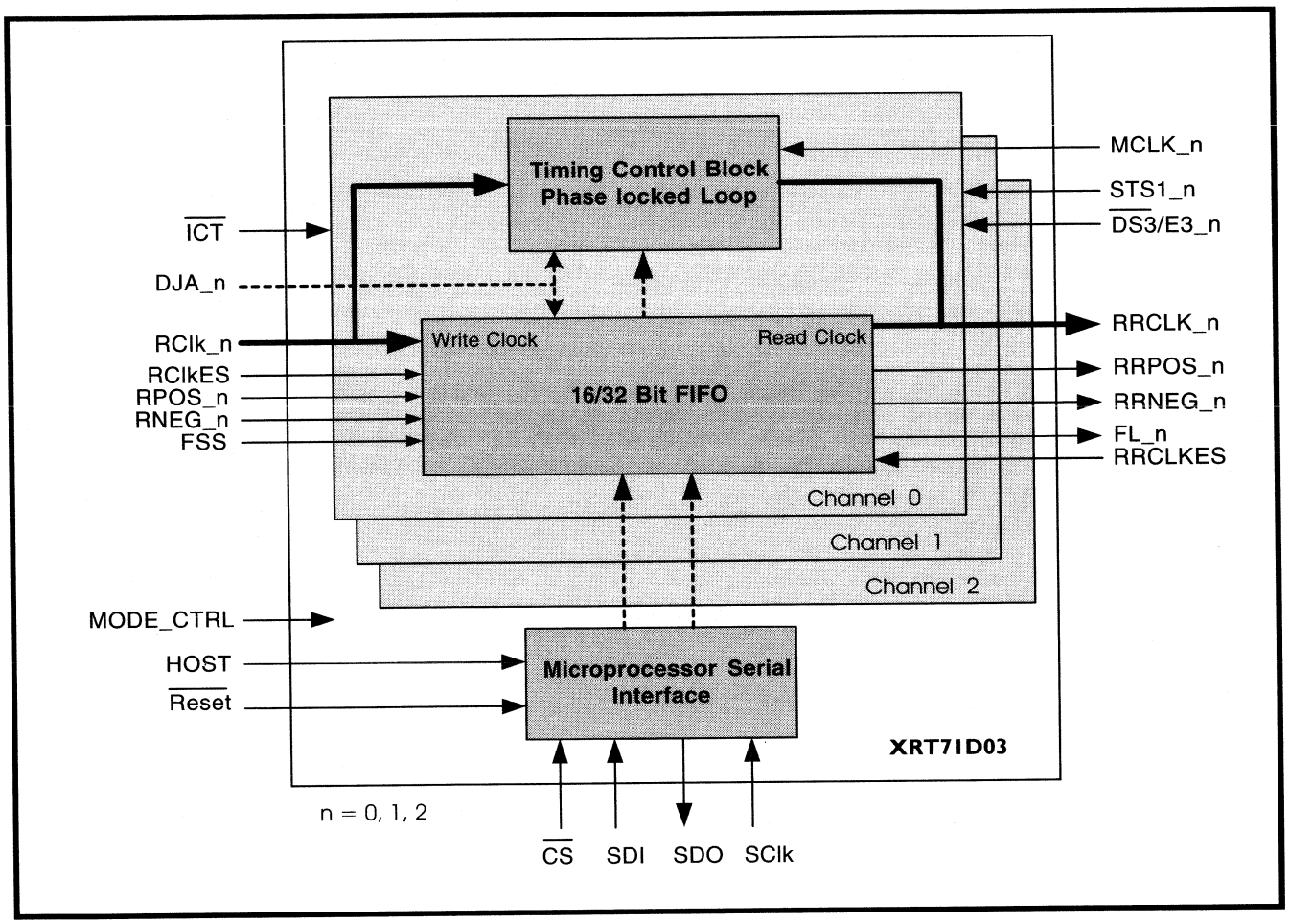
APPLICATIONS

- E3/DS3 Access Equipment.
- STS-SPE to DS3 Mapper
- DSLAMs

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D03IV	64-Lead TQFP	-40°C to +85°C

XRT71D03 BLOCK DIAGRAM



FOUR-CHANNEL DS3/E3/STS-1 JITTER ATTENUATOR, STS-1 TO DS3 DESYNCHRONIZER

REV. 1.1.1

GENERAL DESCRIPTION

The XRT71D04 is a four channel, single chip Jitter Attenuator, that meets the Jitter transfer characteristic requirements specified in the ETSI TBR-24, Bellcore GR-499 and GR-253 standards.

In addition, the XRT71D04 also meets the Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253 and GR-499 standards for Desynchronizing and Pointer adjustments in the DS3 to STS-SPE mapping applications.

FEATURES

- Meets the E3/DS3/STS-1 jitter requirements
- No external components required
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755, GR-499-CORE,1995 GR-253-CORE standards
- Meets output jitter requirement as specified by ETSI TBR24
- Meets the Jitter and Wander specifications described in T1.105.03b,GR-253 and GR-499 standards
- Selectable buffer size of 16 and 32 bits
- Jitter attenuator can be disabled
- Available in a 80 pin TQFP package
- Single 3.3V or 5.0V supply.
- Operates over - 40^0 C to 85^0 C temperature range.

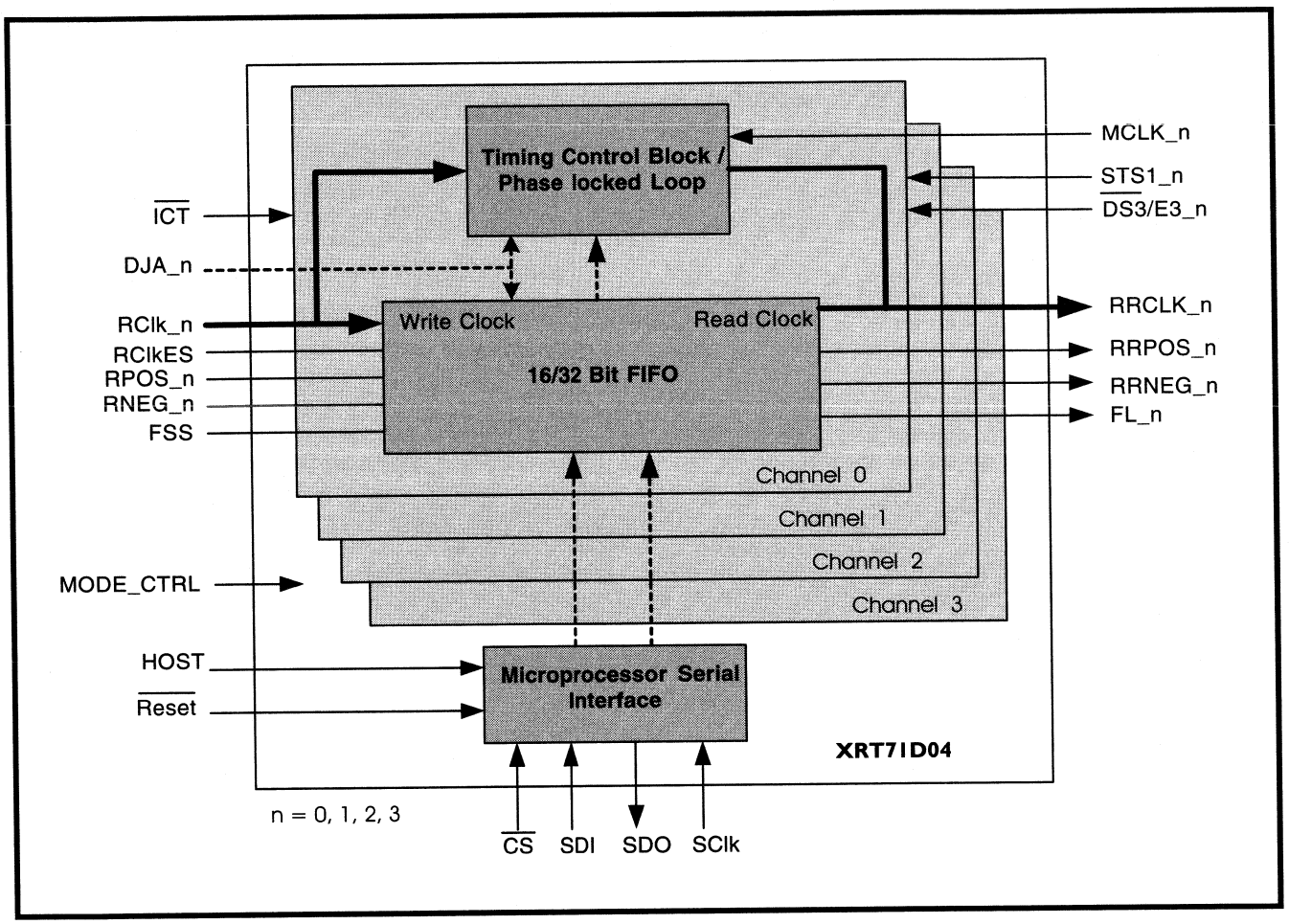
APPLICATIONS

- E3/DS3 Access Equipment
- STS-SPE to DS3 Mapper
- DSLAMs

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D04IV	80-Lead TQFP	-40° C to +85° C

XRT71D04 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT72L13 is a fully integrated, low power, Multiplexer/Framer IC which performs Multiplexing/Demutiplexing of 28 DS1or 21 E1 signals into/from a DS3 signal with either M13 or C-bit parity frame format, performs Clear Channel DS3 Framing, and supports High speed HDLC/LAPD data linking.

The XRT72L13 also contains M12 and M23 bit-interleaving multiplexing/demultiplexing functions with necessary stuffing and destuffing control. Seven internal DS2/G.747 framers are included to support Mux/Demux purposes.

The XRT72L13 contains an integral DS3 Framer which provides Clear Channel DS3 Framing and Error Accumulation in accordance with ANSI/ITU-T specifications.

The XRT72L13 provides the intelligent functions of DS3/DS2 mode control, signaling control, error and alarm reporting and handles the HDLC/LAPD data link through internal registers accessible via an 8-bit parallel, memory mapped, µProcessor interface.

FEATURES

- A fully integrated device that supports:
  - Multiplexing/Demultiplexing Mode
  - Clear Channel DS3 Framer Mode
  - High Speed HDLC Controller Mode
- Supports Multiple Loop-back modes
- Smooths gapped clock signals
- Supports Intel or Motorola PIO µP interfaces
- Available in a 208 pin PQFP package
- Single 3.3V Power Supply
- 5V Tolerant I/O
- Operates over the Industrial Temperature Range

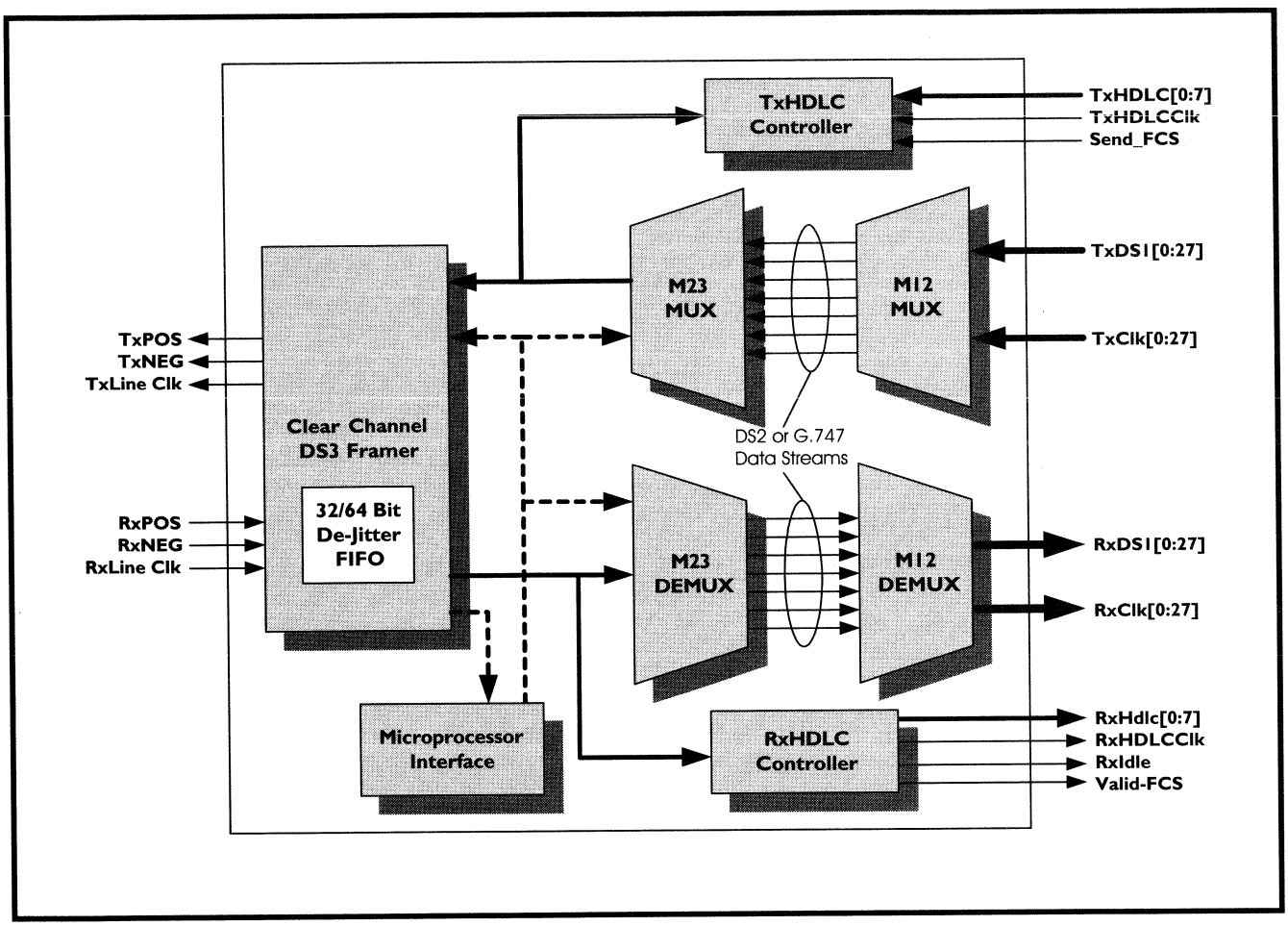
APPLICATIONS

- M13 Multiplexer/Demuliplexer Applications.
- Frame Relay Systems
- Digital Access and Cross Connect Systems
- Local Digital Switch
- Add/Drop Multiplexers
- DS3 Data/Channel Service Units.
- Test Equipment

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L13IQ	208-Lead PQFP	-40°C to +85°C

XRT72L13 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT7234 E3 User Network Interface (UNI) for ATM (Asynchronous Transfer Mode) device is designed to provide the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at E3 rates. This device provides full-duplex data flow between two ATM Layer devices (e.g., ATM Switching equipment) and/or ATM Adaptation Layer (AAL) devices; over a E3 Transport Medium.

FEATURES

- Compliant with UTOPIA Level 1and 2, 8 or 16 Bit, Interface Specification and supports UTOPIA Bus speeds of 25, 33 or 50 MHz
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in the transmit Direction (TxFIFO)
- Contains on-chip Receive OAM Cell Buffer for reception, filtering and processing of selected User and OAM Cells
- Supports PLCP or ATM Direct Mapping modes
- Supports the ITU-T G.832 Framing Format
- Supports Line and Cell Loop-backs
- Interfaces to 8 or 16 Bit wide Motorola and Intel µPs and µCs
- +5V Power Supply, CMOS Technology
- Operates over the Industrial Temperature Range (-40°C to +85°C)
- Available in a 160 pin PQFP Packages

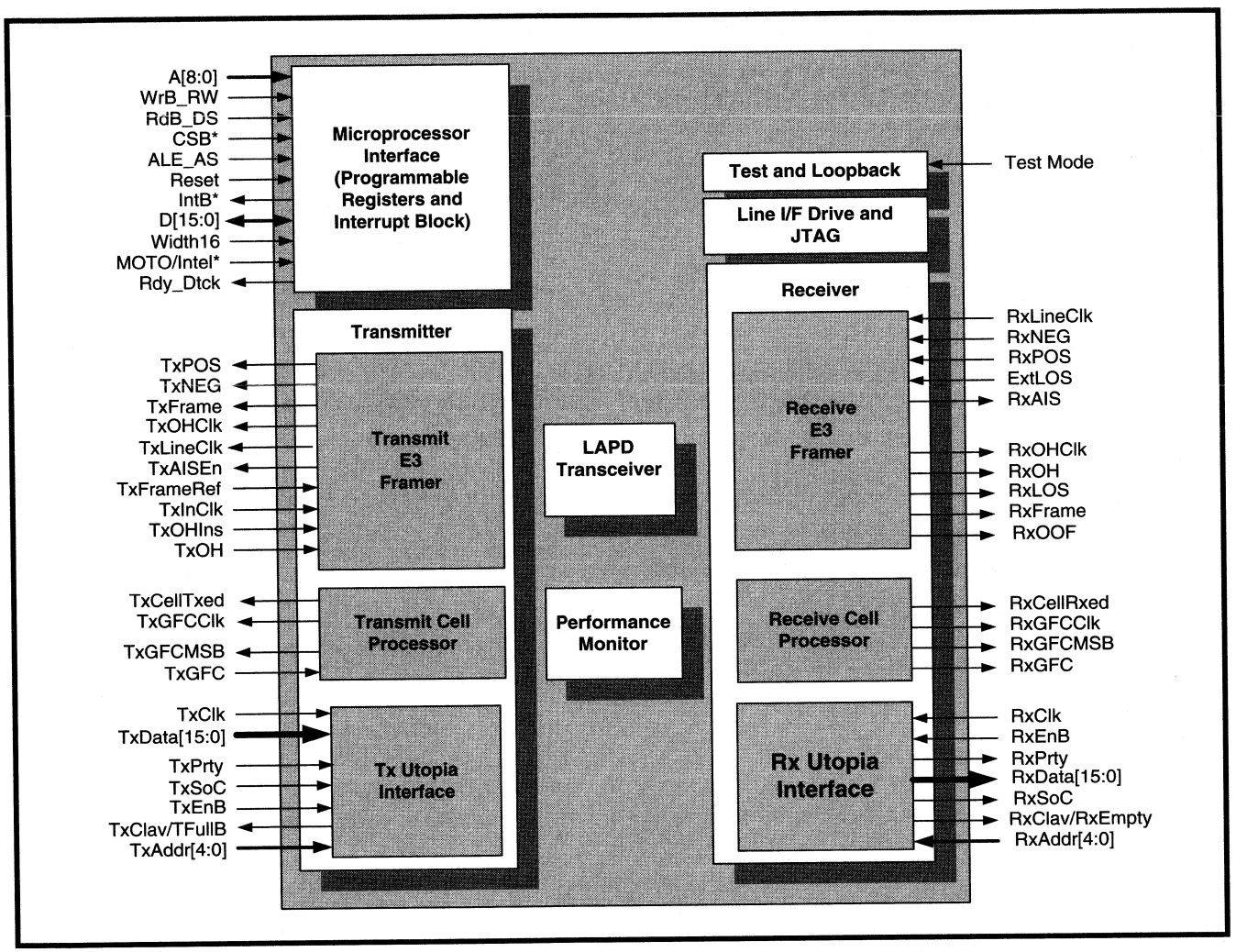
APPLICATIONS

- Private User Network Interfaces
- ATM Switches
- ATM Routers and Bridges

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT7234IQ	160-Lead PQFP	-40°C to +85°C

XRT7234 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT7245 DS3 ATM User Network Interface (UNI) device is designed to provide the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3 rates. This device provides full-duplex data flow between two ATM Layer devices (e.g., ATM Switching equipment) and/or ATM Adaptation Layer (AAL) devices; over a DS3 Transport Medium.

The XRT7245 DS3 UNI for ATM incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive functional sections.

FEATURES

- Compliant with UTOPIA Level 1and 2, 8 or 16 Bit, Interface Specification and supports UTOPIA Bus operating at 25, 33 or 50 MHz
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in the transmit Direction (TxFIFO)
- Contains on-chip Receive OAM Cell Buffer for reception, filtering and processing of selected User and OAM Cells
- Supports PLCP or ATM Direct Mapping modes
- Supports M13 and C-Bit Parity Framing Formats
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 or 16 Bit wide Motorola and Intel µPs and µCs
- Available in 160-pin PQFP Package

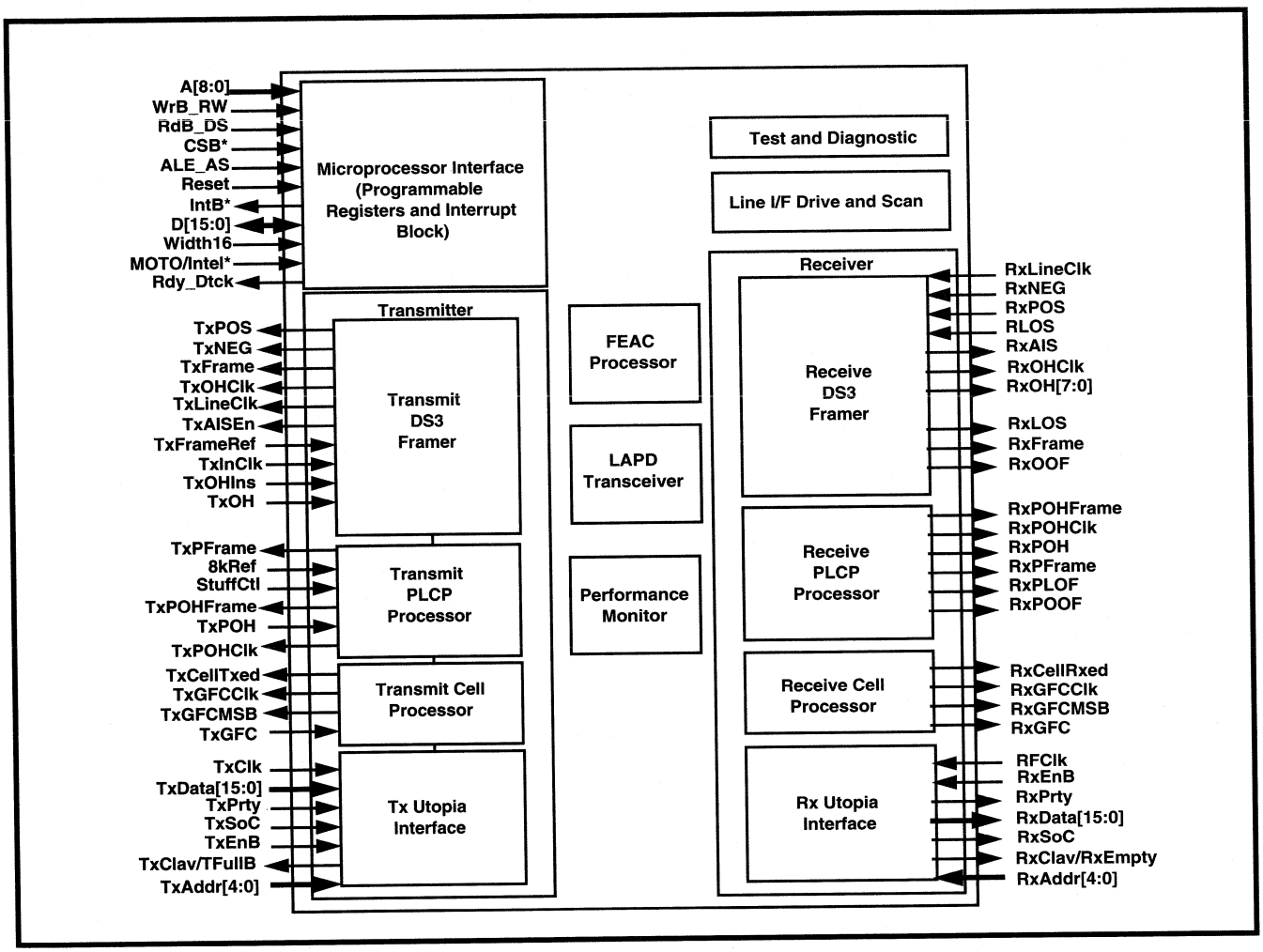
APPLICATIONS

- Private User Network Interfaces
- ATM Switches
- ATM Routers and Bridges
- ATM Concentrators

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT7245IQ	160-Lead PQFP	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM OF THE XRT7245 DS3 UNI



GENERAL DESCRIPTION

The XRT7250 DS3/E3 Framer IC is designed to accept "User Data" from the Terminal Equipment and insert this data into the "payload" bit-fields within an "outbound" DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an "inbound" DS3/E3 Data Stream (from the Remote Terminal Equipment) and extract out the "User Data".

The XRT7250 DS3/E3 Framer is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT7250 DS3/E3 Framer IC consists of four sections.

The Transmit Section, includes a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit E3/DS3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Section, consists of a Receive LIU Interface, a Receive E3/DS3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Section consists of a large number of "Reset-upon-Read" and "Read-Only" registers that contain cumulative and "one-second" statistics that reflect the performance/health of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 100 Pin PQFP package
- Operating Temperature -40°C to +85°C

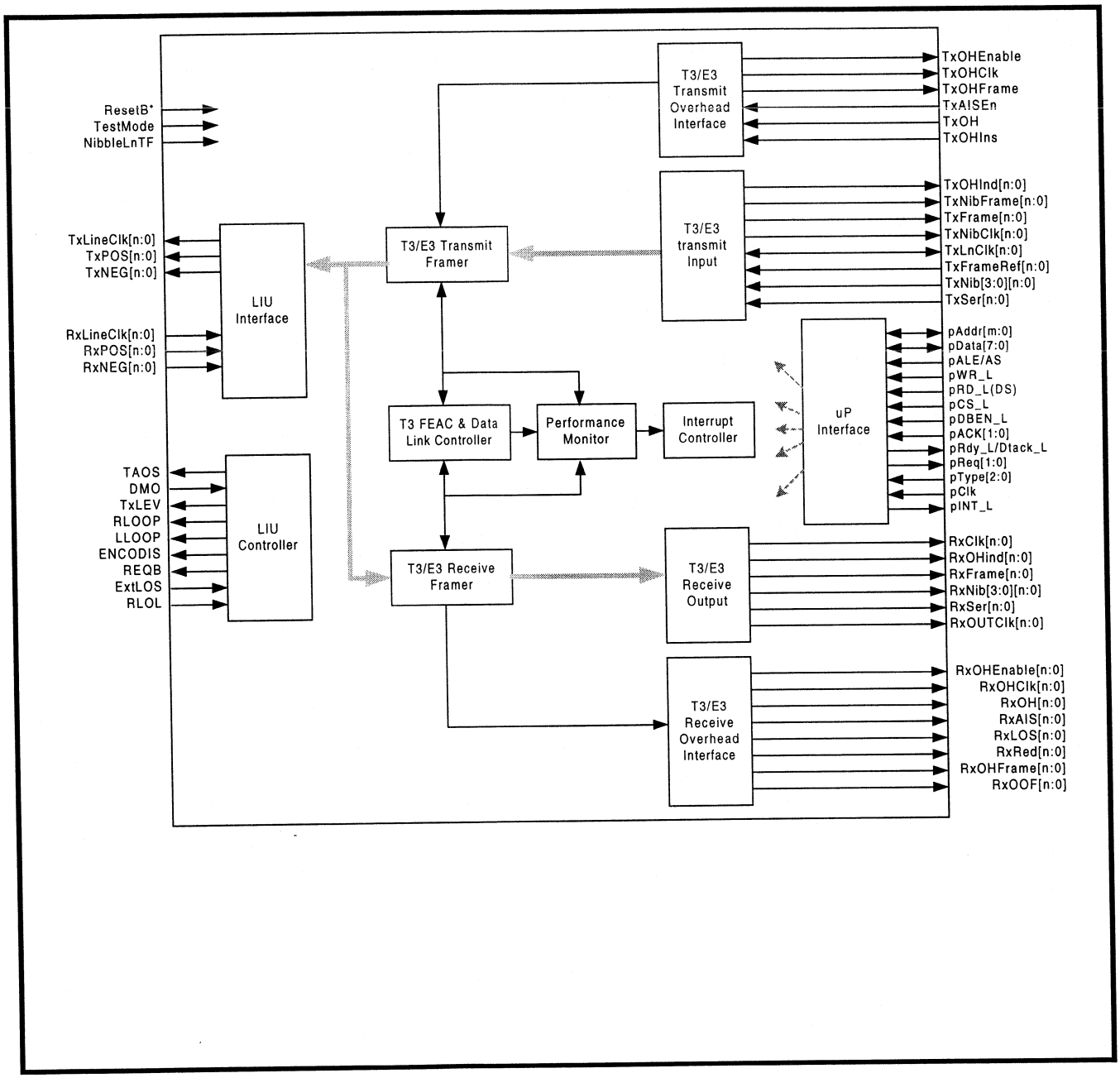
APPLICATIONS

- Interface to DS3 or E3 Networks
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals

ORDERING INFORMATION

Operating Part No.	Package	Temperature Range
XRT7250IQ	100-Lead PQFP (24 x 18 x 3 mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT7250 DS3/E3 FRAMER



GENERAL DESCRIPTION

The XRT72L50, single Channel DS3/E3 Framer IC is designed to accept "User Data" from the Terminal Equipment and insert this data into the "payload" bit-fields within an "outbound" DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an "inbound" DS3/E3 Data Stream (from the Remote Terminal Equipment) and extract out the "User Data".

The XRT72L50 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT72L50 DS3/E3 Framer IC consists of a Transmit section, Receiver section, Performance Monitor Section and a Microprocessor interface.

The Transmit Section, includes a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Section, consists of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of "Reset-upon-Read" and "Read-Only" registers that contain cumulative and "one-second" statistics that reflect the performance/health of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 1 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 100 Pin PQFP package
- 3.3V Power Supply with 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

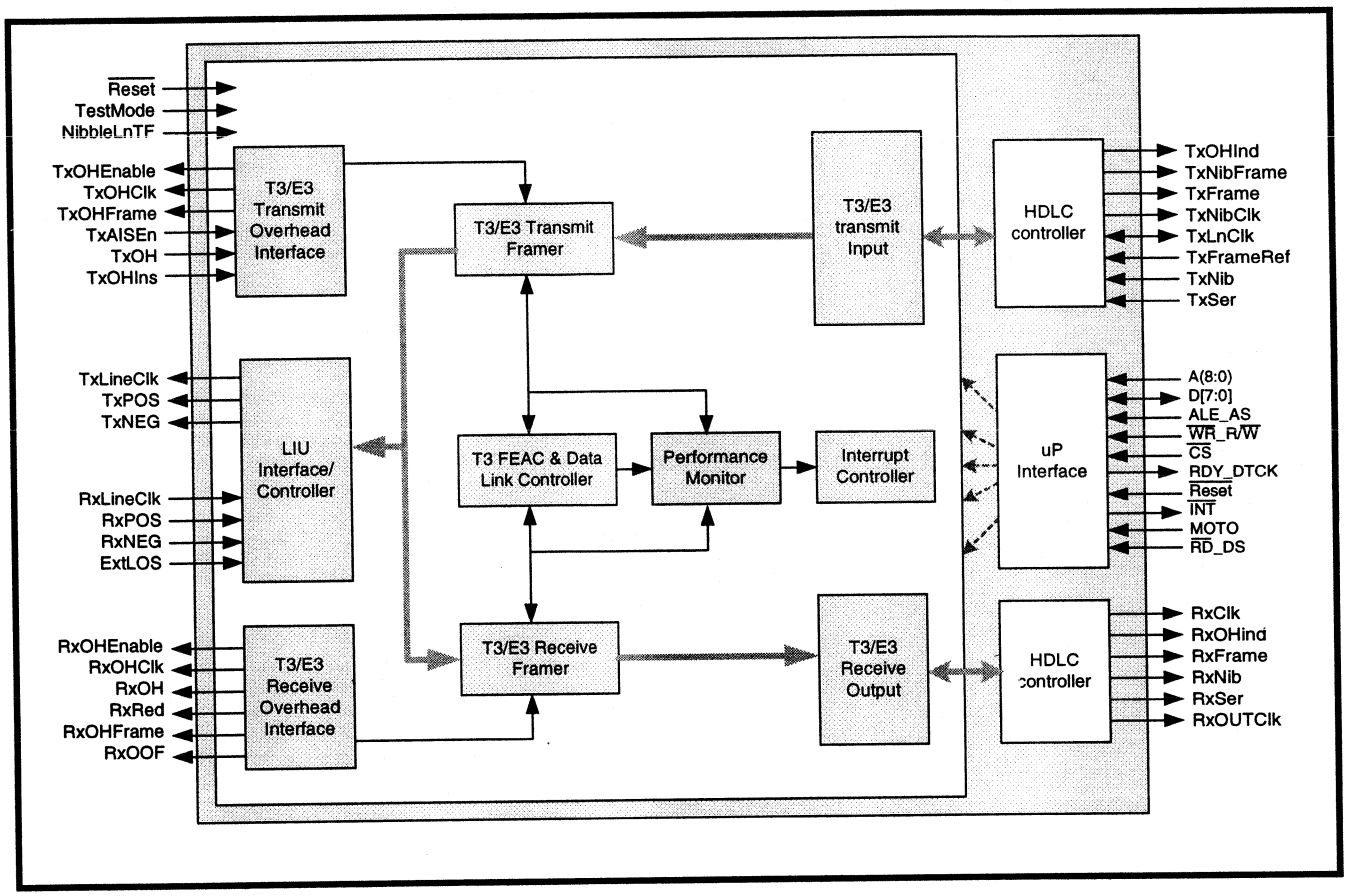
APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

ORDERING INFORMATION

OPERATING PART NO.	PACKAGE	TEMPERATURE RANGE
XRT72L50IQ	100-Lead PQFP(14 x 20mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT72L50



TWO-CHANNEL DS3/E3 FRAMER WITH HDLC CONTROLLER

GENERAL DESCRIPTION

The XRT72L52, 2 Channel DS3/E3 Framer IC is designed to accept "User Data" from the Terminal Equipment and insert this data into the "payload" bit-fields within an "outbound" DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an "inbound" DS3/E3 Data Stream (from the Remote Terminal Equipment) and extract out the "User Data".

The XRT72L52 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT72L52 DS3/E3 Framer IC consists of two Transmit sections, two Receiver sections, two Performance Monitor Sections and a Microprocessor interface.

The Transmit Sections, include a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Sections, consist of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of "Reset-upon-Read" and "Read-Only" registers that contain cumulative and "one-second" statistics that reflect the performance/health of the two channels of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 2 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 160 Pin PQFP package
- 3.3V Power Supply with 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

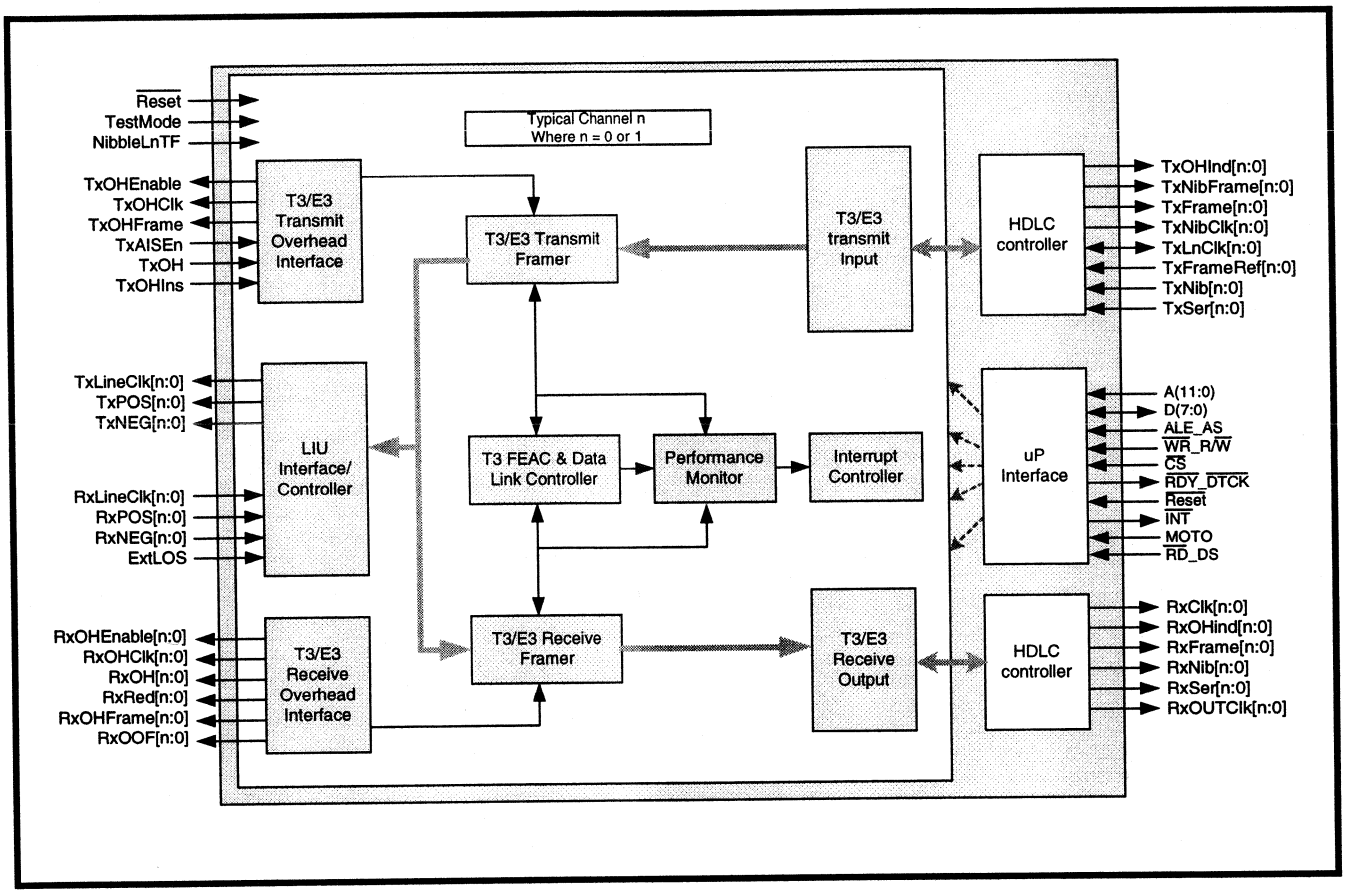
APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

ORDERING INFORMATION

Operating Part No.	Package	Temperature Range
XRT72L52IQ	160-Lead PQFP (28 x 28mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT72L52



THREE-CHANNEL DS3/E3 FRAMER WITH HDLC CONTROLLER

GENERAL DESCRIPTION

The XRT72L53, 3 Channel DS3/E3 Framer IC is designed to accept User Data from the Terminal Equipment and insert this data into the Payload bit-fields within an Outbound DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an Inbound DS3/E3 Data Stream (from the Remote Terminal Equipment) and extract out the User Data.

The XRT72L53 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 (November 1995 and October 1998 Revisions) Framing Formats.

The XRT72L53 DS3/E3 Framer IC consists of three Transmit sections, three Receiver sections, three Performance Monitor Sections and a Microprocessor interface.

Each Transmit Sections, include a Transmit Payload Data Input Interface block, a Transmit Overhead Data Input Interface block, a Transmit FEAC and LAPD Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Sections, consist of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive FEAC and LAPD Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of Reset-upon-Read and Read-Only registers that contain cumulative and One-Second statistics that reflect the performance/health of the three channels of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 3 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 272 Ball PBGA package
- 3.3V Power Supply, 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

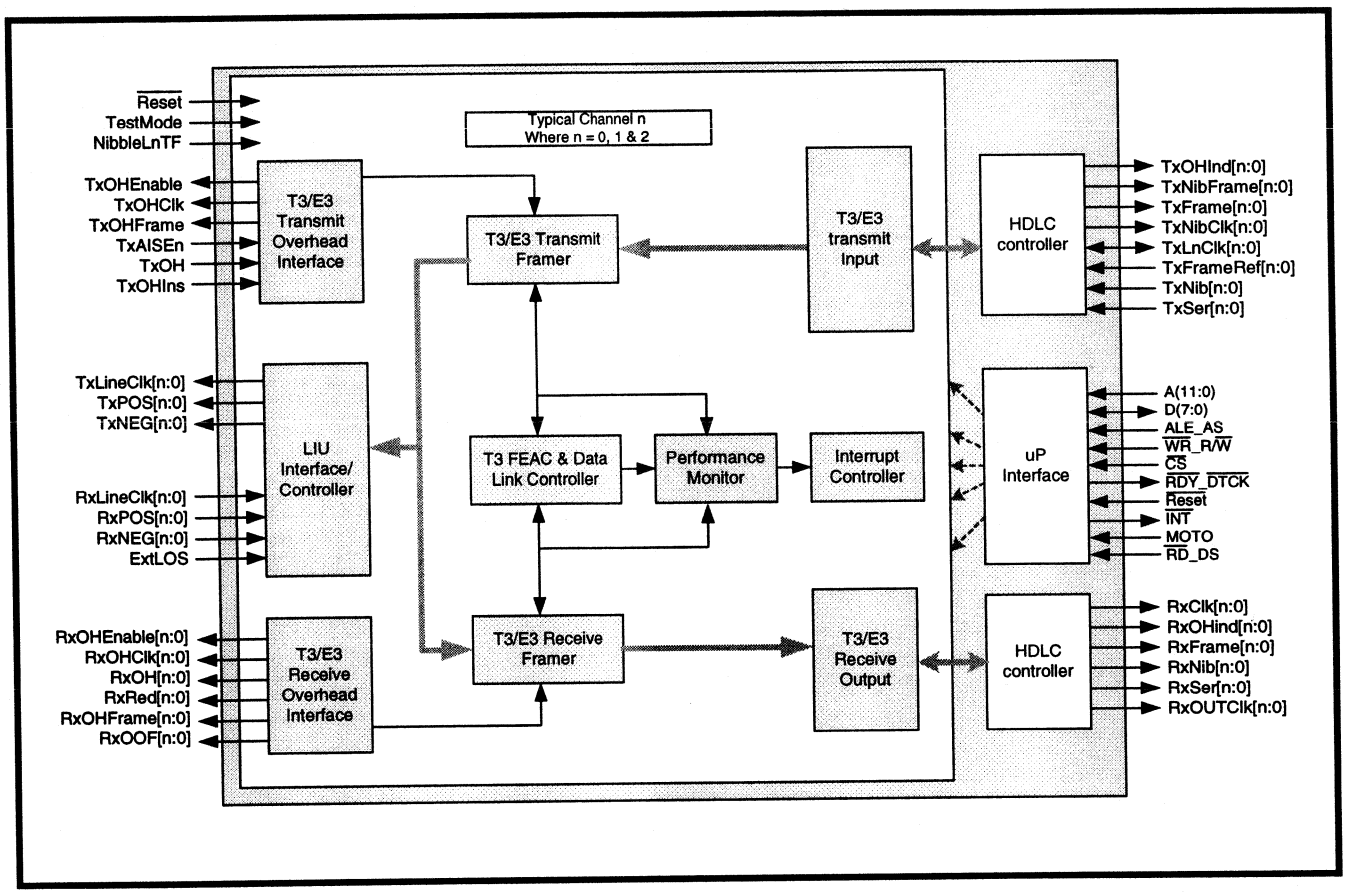
APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

ORDERING INFORMATION

Operating Part No.	Package	Temperature Range
XRT72L53IB	272 Ball PBGA (27 x 27mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT72L53



FOUR-CHANNEL DS3/E3 FRAMER WITH HDLC CONTROLLER

GENERAL DESCRIPTION

The XRT72L54, 4 Channel DS3/E3 Framer IC is designed to accept "User Data" from the Terminal Equipment and insert this data into the "payload" bit-fields within an "outbound" DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an "inbound" DS3/E3 Data Stream (from the Remote Terminal Equipment) and extract out the "User Data".

The XRT72L54 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT72L54 DS3/E3 Framer IC consists of Four Transmit sections, Four Receiver sections, Four Performance Monitor Sections and a Microprocessor interface.

The Transmit Sections, include a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Sections, consist of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of "Reset-upon-Read" and "Read-Only" registers that contain cumulative and "one-second" statistics that reflect the performance/health of the Four channels of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 6 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 272 Ball PBGA package
- 3.3V Power Supply, 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

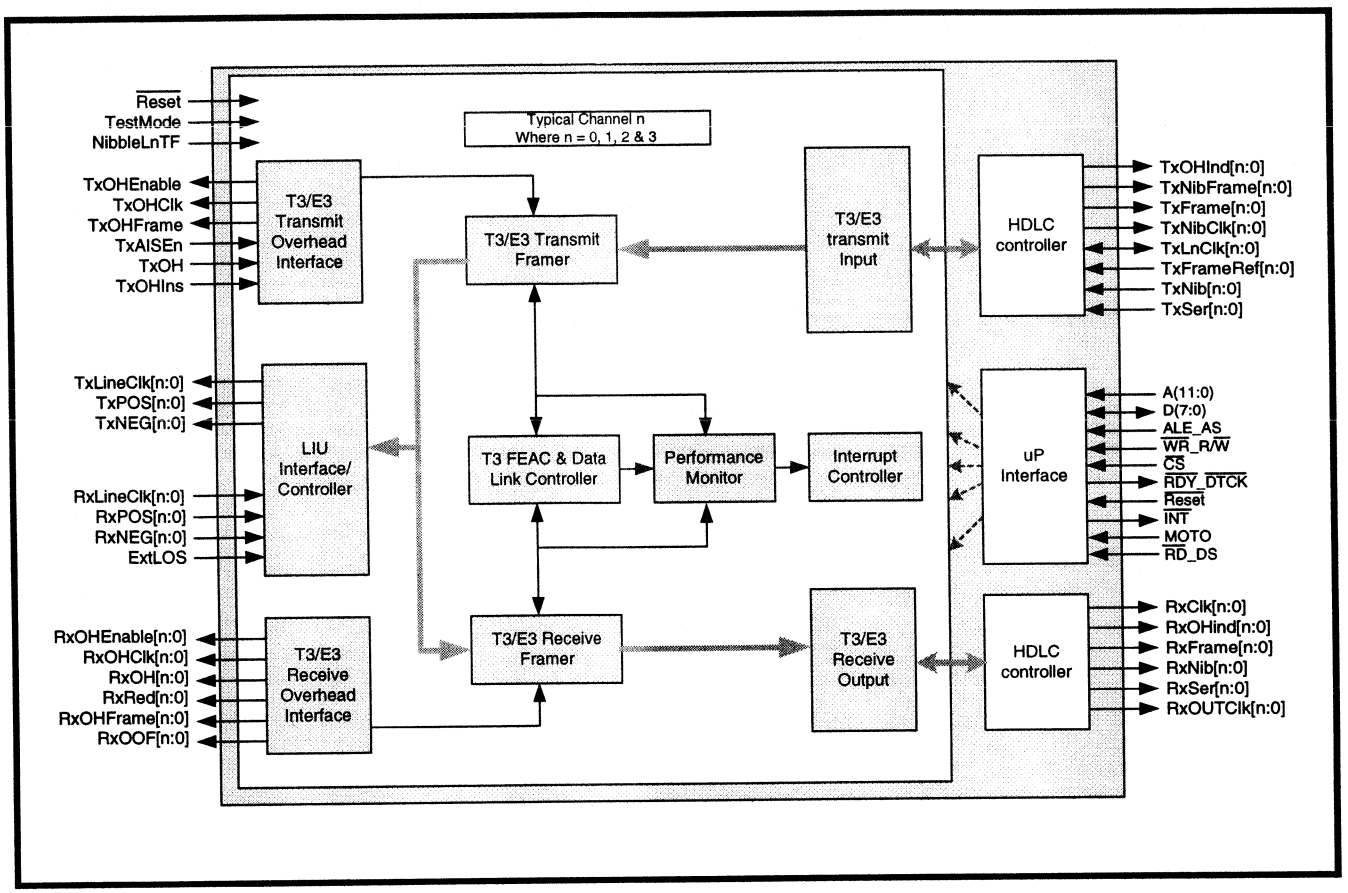
APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

ORDERING INFORMATION

Operating Part No.	Package	Temperature Range
XRT72L54IB	272 Ball PBGA (27 x 27mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT72L54



SIX-CHANNEL DS3/E3 FRAMER WITH HDLC CONTROLLER

GENERAL DESCRIPTION

The XRT72L56, 6 Channel DS3/E3 Framer is designed to accept "User Data" from the Terminal Equipment and insert this data into the "payload" bit-fields within an "outbound" DS3/E3 Data Stream.

The XRT72L56 DS3/E3 Framer support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) . The Framer will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

In addition, XRT72L56 has 6 independent high speed HDLC controllers both on the receive and transmit data paths which can be optionally configured to support Framer Relay applications.

The Transmit Sections, include a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Sections, consist of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of "Reset-upon-Read" and "Read-Only" registers that contain cumulative and "one-second" statistics that reflect the performance/status of the channels.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- Per Channel High Speed HDLC Controllers.
- Interfaces to all Popular Microprocessors
- Extensive Performance Monitoring support.
- Available in a 388 Ball PBGA package
- 3.3V Power Supply with 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

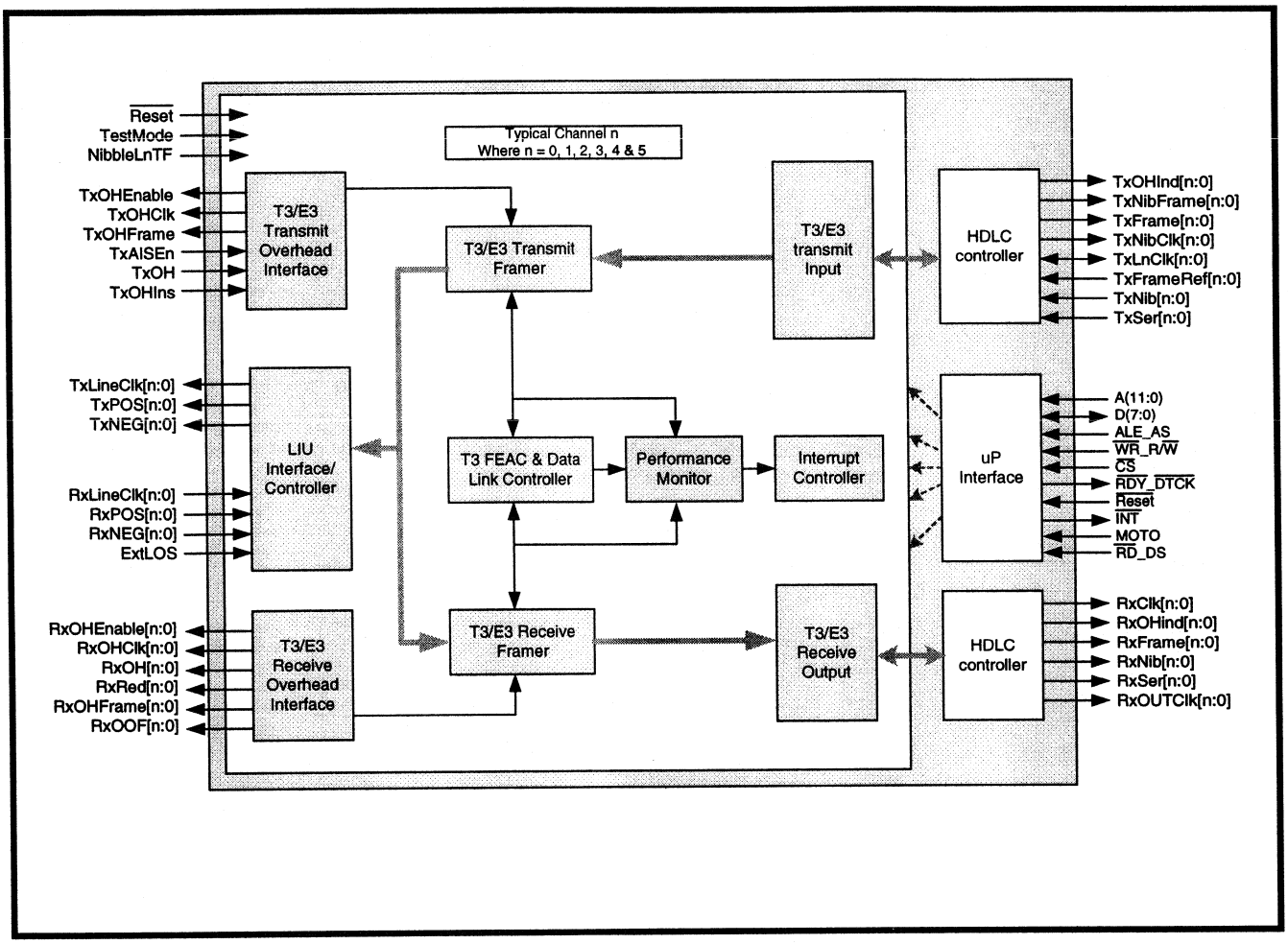
APPLICATIONS

- Digital Cross Connects
- CSU/DSU Equipment.
- ADD/Drop Multiplexers
- DS3/E3 Frame Relay Equipment

ORDERING INFORMATION

Operating Part No.	Package	Temperature Range
XRT72L56IB	388 Ball PBGA (35 x 35mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT72L56



EIGHT-CHANNEL DS3/E3 FRAMER WITH HDLC CONTROLLER

GENERAL DESCRIPTION

The XRT72L58 Octal DS3/E3 Framer is designed to accept "User Data" from the Terminal Equipment and insert this data into the "payload" bit-fields within an "outbound" DS3/E3 Data Stream. Further, the Framer is also designed to receive an "inbound" DS3/E3 Data Stream (from the Remote Terminal Equipment) and extract out the "User Data".

The XRT72L58 DS3/E3 Framer is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT72L58 DS3/E3 Framer consists of Eight Transmit sections, Eight Receiver sections, Eight Performance Monitor Sections and a Microprocessor interface.

The Transmit Sections, include a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Sections, consist of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of "Reset-upon-Read" and "Read-Only" registers that contain cumulative and "one-second" statistics that reflect the performance/health of the Eight channels of the Framer/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 8 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 388 Ball PBGA package
- 3.3V Power Supply with 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

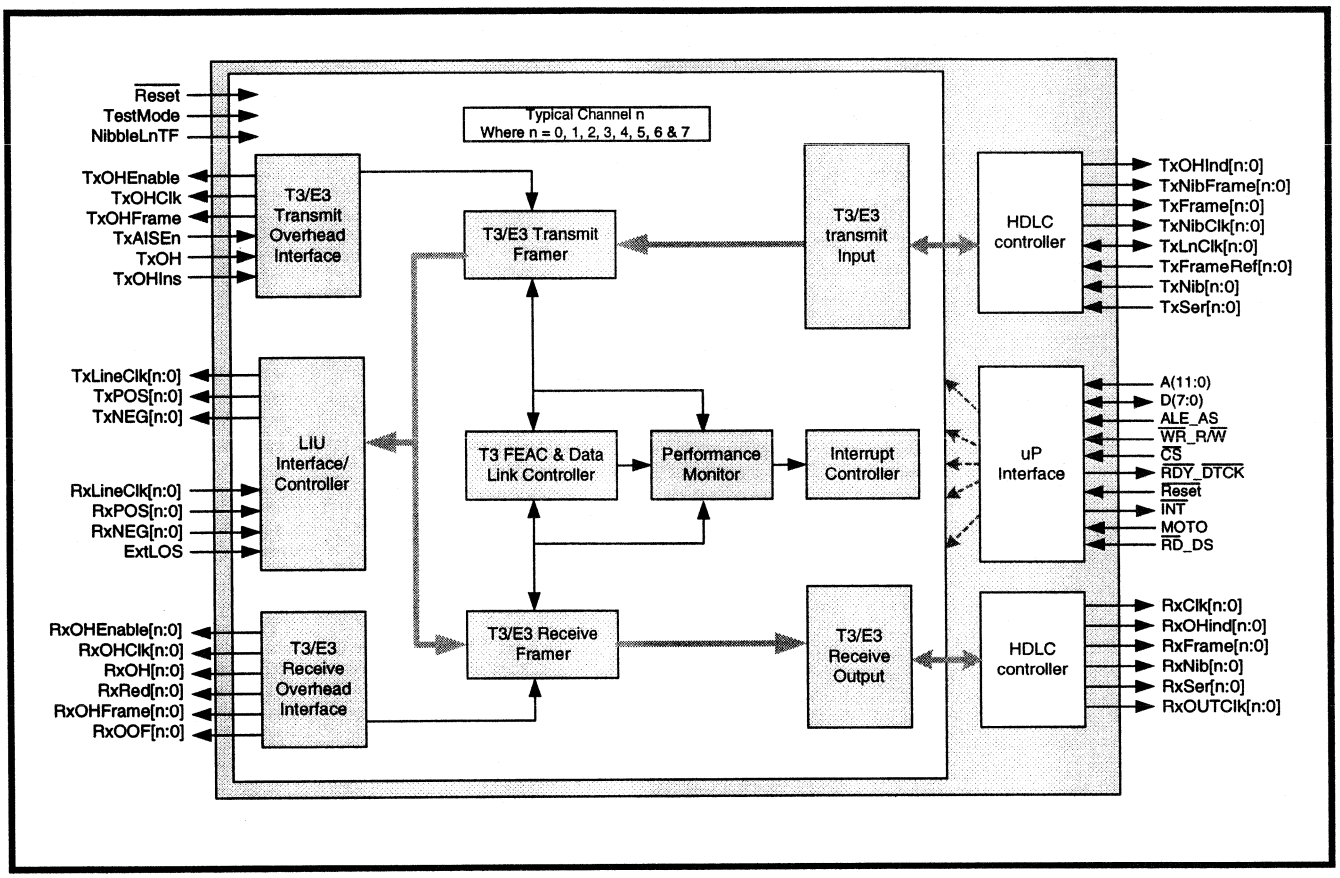
APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

ORDERING INFORMATION

Operating Part No.	Package	Temperature Range
XRT72L58IB	388 Ball PBGA (35 x 35mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT72L58



GENERAL DESCRIPTION

The XRT72L71 DS3 ATM User Network Interface (UNI)/Clear-Channel Framer is designed to function as either a DS3 ATM UNI or Clear channel framer. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for both the public and private networks at DS3 rates. For Clear-Channel framer applications, this device supports the transmission and reception of "user data" via the DS3 payload bits.

The XRT72L71incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive sections.

APPLICATIONS

- Private User Network Interfaces
- ATM Switches
- ATM Concentrators
- DSLAM Equipment
- DS3 Frame Relay Equipment

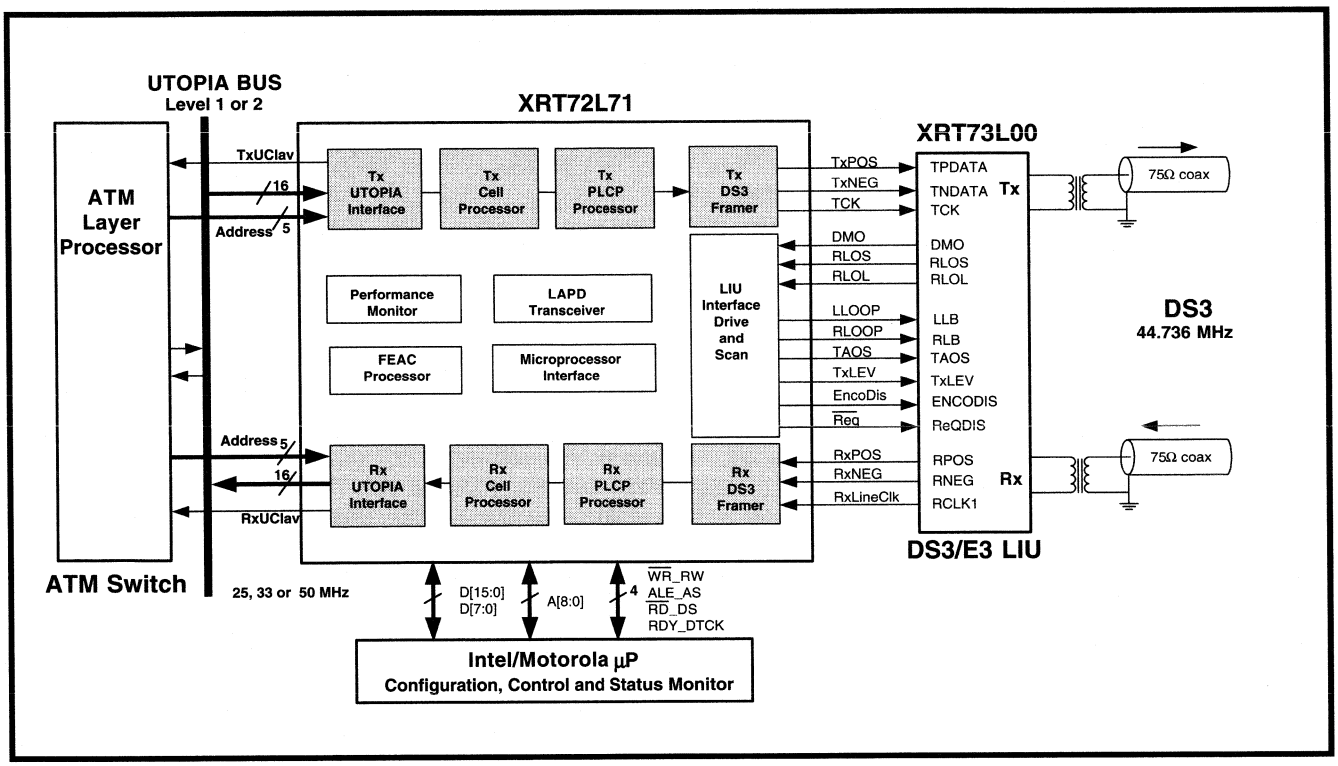
FEATURES

- Compliant with UTOPIA Level 1 and 2 with 8 or 16 Bit Interface Specification and supports UTOPIA Bus speeds of up to 50 MHz
- Contains on-chip 16 cell FIFO in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit OAM Cell buffer and a 108 byte Receive OAM cell buffer, for transmission, reception and processing of OAM cells.
- Supports PLCP or ATM Direct Mapping modes
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3 Clear Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Local, Remote-Line, Cell, and PLCP Loop-backs
- Interfaces to 8 or 16 Bit wide Motorola and Intel µPs
- Low power 3.3V, 5V input tolerant, CMOS
- 160 pin PQFP Package
- 3 and 4 Channel Version also Available

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L71IQ	160-Lead PQFP	-40° C to +85° C

XRT72L71 BLOCK DIAGRAM



THREE-CHANNEL DS3 ATM UNI/CLEAR CHANNEL FRAMER

GENERAL DESCRIPTION

The XRT72L73 Three Channel DS3 ATM User Network Interface (UNI)/Clear Channel Framer is designed to function as either a DS3 ATM UNI or Clear channel framer. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sublayers) interface for both the public and private networks at DS3 rates. For Clear-Channel framer applications, this device supports the transmission and reception of "user data" via the DS3 payload bits.

The XRT72L73 incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive sections.

APPLICATIONS

- Private User Network Interfaces
- ATM Switches
- ATM Concentrators
- DSLAM Equipment
- DS3 Frame Relay Equipment

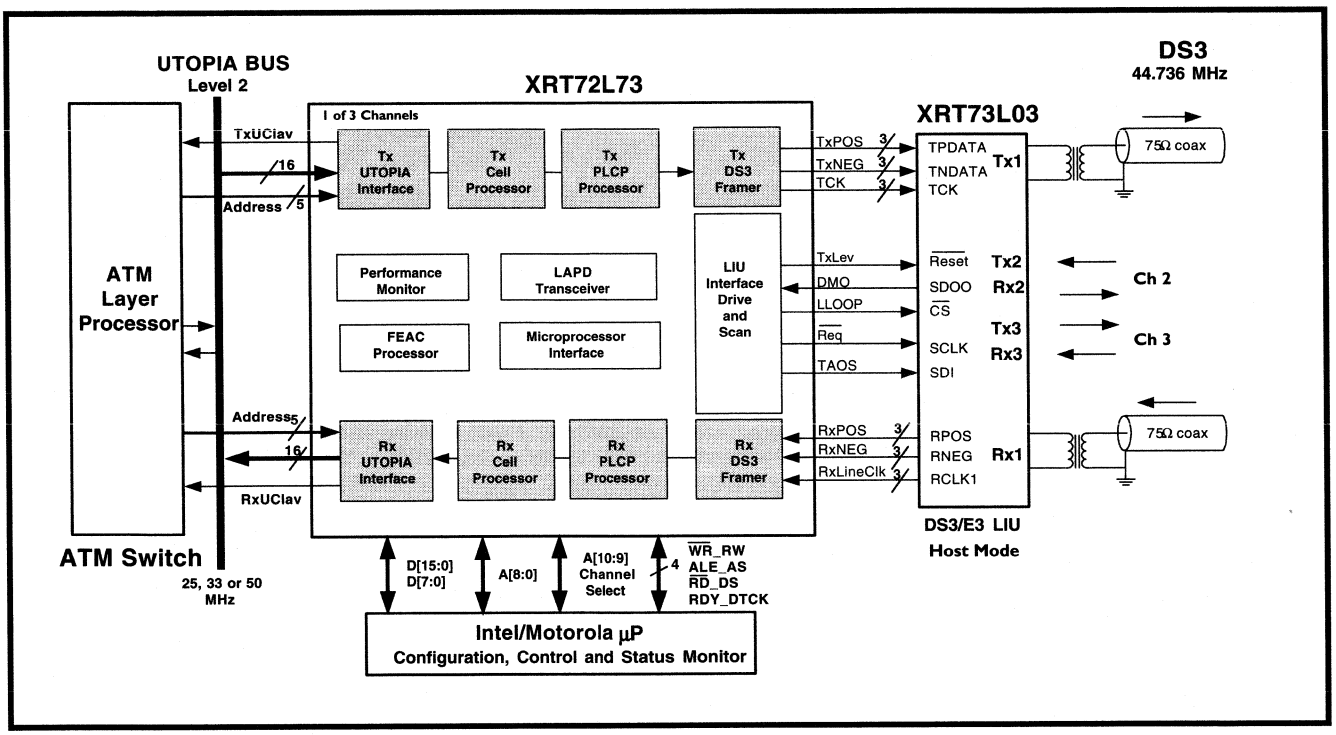
FEATURES

- Compliant with UTOPIA Level 1 and 2 with 8 or 16 Bit Interface Specification and supports UTOPIA Bus speeds of up to 50 MHz
- Contains on-chip 16 cell FIFO in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit OAM Cell buffer and a 108 byte Receive OAM cell buffer, for transmission, reception and processing of OAM cells.
- Supports PLCP or ATM Direct Mapping modes
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3 Clear Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Local, Remote-Line, Cell, and PLCP Loop-backs
- Interfaces to 8 or 16 Bit wide Motorola and Intel µPs
- Low power 3.3V, 5V input tolerant, CMOS
- 352 ball PBGA Package
- 1 and 3 channel versions also available
- 1 and 3 channel versions also available

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L73IB	352 Ball PBGA (35 x 35mm)	-40°C to +85°C

XRT72L73 BLOCK DIAGRAM



FOUR-CHANNEL DS3 ATM UNI/CLEAR CHANNEL FRAMER

GENERAL DESCRIPTION

The XRT72L74 Four Channel DS3 ATM User Network Interface (UNI)/Clear Channel Framer is designed to function as either a DS3 ATM UNI or Clear channel framer. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sublayers) interface for both the public and private networks at DS3 rates. For Clear-Channel framer applications, this device supports the transmission and reception of "user data" via the DS3 payload bits.

The XRT72L74 incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive sections.

APPLICATIONS

- Private User Network Interfaces
- ATM Switches
- ATM Concentrators
- DSLAM Equipment
- DS3 Frame Relay Equipment

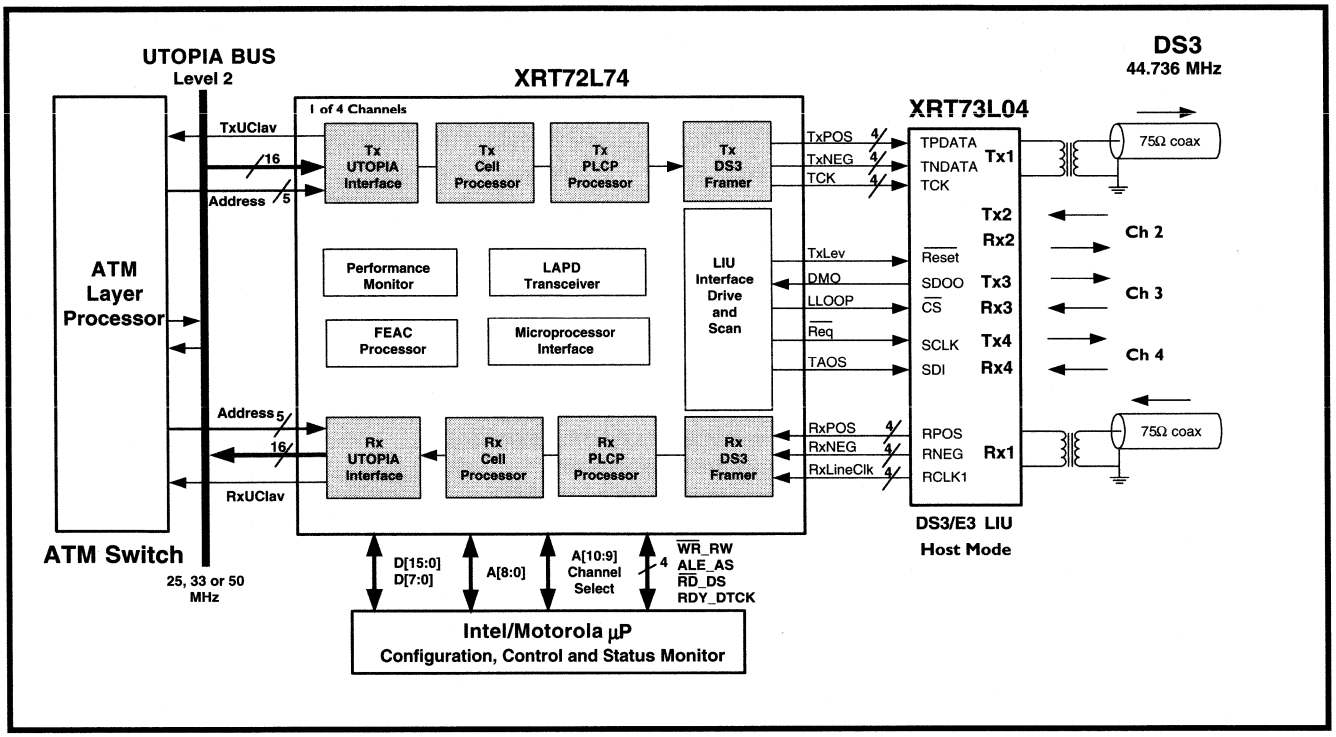
FEATURES

- Compliant with UTOPIA Level 1 and 2 with 8 or 16 Bit Interface Specification and supports UTOPIA Bus speeds of up to 50 MHz
- Contains on-chip 16 cell FIFO in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit OAM Cell buffer and a 108 byte Receive OAM cell buffer, for transmission, reception and processing of OAM cells.
- Supports PLCP or ATM Direct Mapping modes
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3 Clear Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Local, Remote-Line, Cell, and PLCP Loop-backs
- Interfaces to 8 or 16 Bit wide Motorola and Intel µPs
- Low power 3.3V, 5V input tolerant, CMOS
- 352 ball PBGA Package
- 1 and 3 channel versions also available

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L74IB	352 Ball PBGA (35 x 35mm)	-40°C to +85°C

XRT72L74 BLOCK DIAGRAM



DS3/SONET STS-1 INTEGRATED LINE RECEIVER

GENERAL DESCRIPTION

The XRT7295 DS3/SONET STS-1 integrated line receiver is a fully integrated receive interface that terminates a bipolar DS3 (44.736Mbps) or SONET STS-1 (51.84Mbps) signal transmitted over coaxial cable.

The device also provides the functions of receive equalization (optional), automatic-gain control (AGC), clock-recovery and data retiming, loss-of-signal and loss-of-frequency-lock detection. The digital system interface is dual-rail, with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable distances of 0 to 450ft. from the cross-connect frame to the device. The receive input has a variable input sensitivity control, providing three different sensitivity settings, to adapt longer cables. High input sensitivity allows for significant amounts of flat loss within the system. Figure 1 shows the block diagram of the device.

The XRT7295 device is manufactured using linear CMOS technology. The XRT7295 is available in either a 20-pin plastic DIP or 20-pin plastic SOJ package for surface mounting.

Two versions of the chip are available, one is for either DS3 or STS-1 operation (the XRT7295, this data sheet), and the other is for E3 operation (the XRT7295E, refer to the XRT7295E data sheet). Both versions are pin compatible.

For either DS3 or STS-1, an input reference clock at 44.736MHz or 51.84MHz provides the frequency reference for the device.

FEATURES

- Fully Integrated Receive Interface for DS3 and STS-1 Rate Signals
- Integrated Equalization (Optional) and Timing Recovery
- Loss-of-Signal and Loss-of-Lock Alarms
- Variable Input Sensitivity Control
- 5V Power Supply
- Pin Compatible with XRT7295E
- Companion Device to T7296 Transmitter

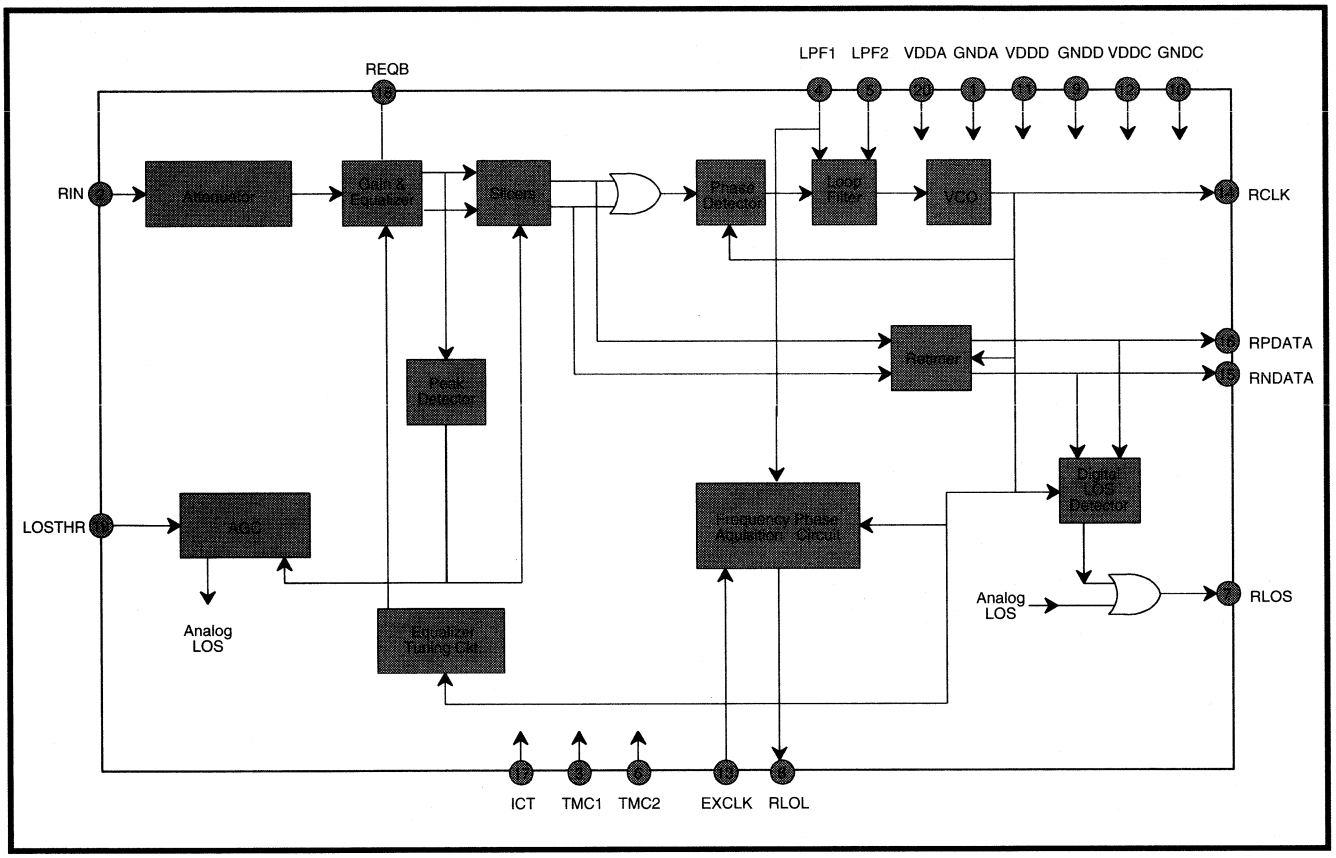
APPLICATIONS

- Interface to DS-3 Networks
- Digital Cross-Connect Systems
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals

ORDERING INFORMATION

Operating Part No.	Package	Temperature Range
XRT7295IP	20-Lead 300 Mil PDIP	-40°C to +85°C°
XRT7295IW	20-Lead 300 Mil JEDEC SOJ	-40°C to +85°C

XRT7295 BLOCK DIAGRAM



E3 (34.368 MBPS) INTEGRATED LINE RECEIVER

GENERAL DESCRIPTION

The XRT7295E E3 Integrated Line Receiver is a fully integrated receive interface that terminates a bipolar E3 (34.3684Mbps) signal transmitted over coaxial cable. This device can be used with the XRT7296 Integrated Line Transmitter.

The device provides the functions of receive equalization (optional), automatic-gain control (AGC), clock-recovery and data retiming, loss-of-signal and loss-of-frequency- lock detection. The digital system interface is dual-rail, with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable losses of 0 to 15 dB. The receive input has a variable input sensitivity control, providing three different sensitivity settings. High input sensitivity allows for significant amounts of flat loss or for use with input signals at the monitor level. Figure 1 shows the block diagram of the device.

The XRT7295E device is manufactured by using linear CMOS technology. The XRT7295E is available in either a 20-pin plastic DIP or 20-pin plastic SOJ package for surface mounting. A pin compatible version is available for DS3 or STS-1 applications. Please refer to the XRT7295 datasheet.

FEATURES

- Fully Integrated Receive Interface for E3 Signals
- Integrated Equalization (Optional) and Timing Recovery
- Loss-of-Signal and Loss-of-Lock Alarms
- Variable Input Sensitivity Control
- 5V Power Supply
- Compliant with G.703, G.775 and G.824 Specifications

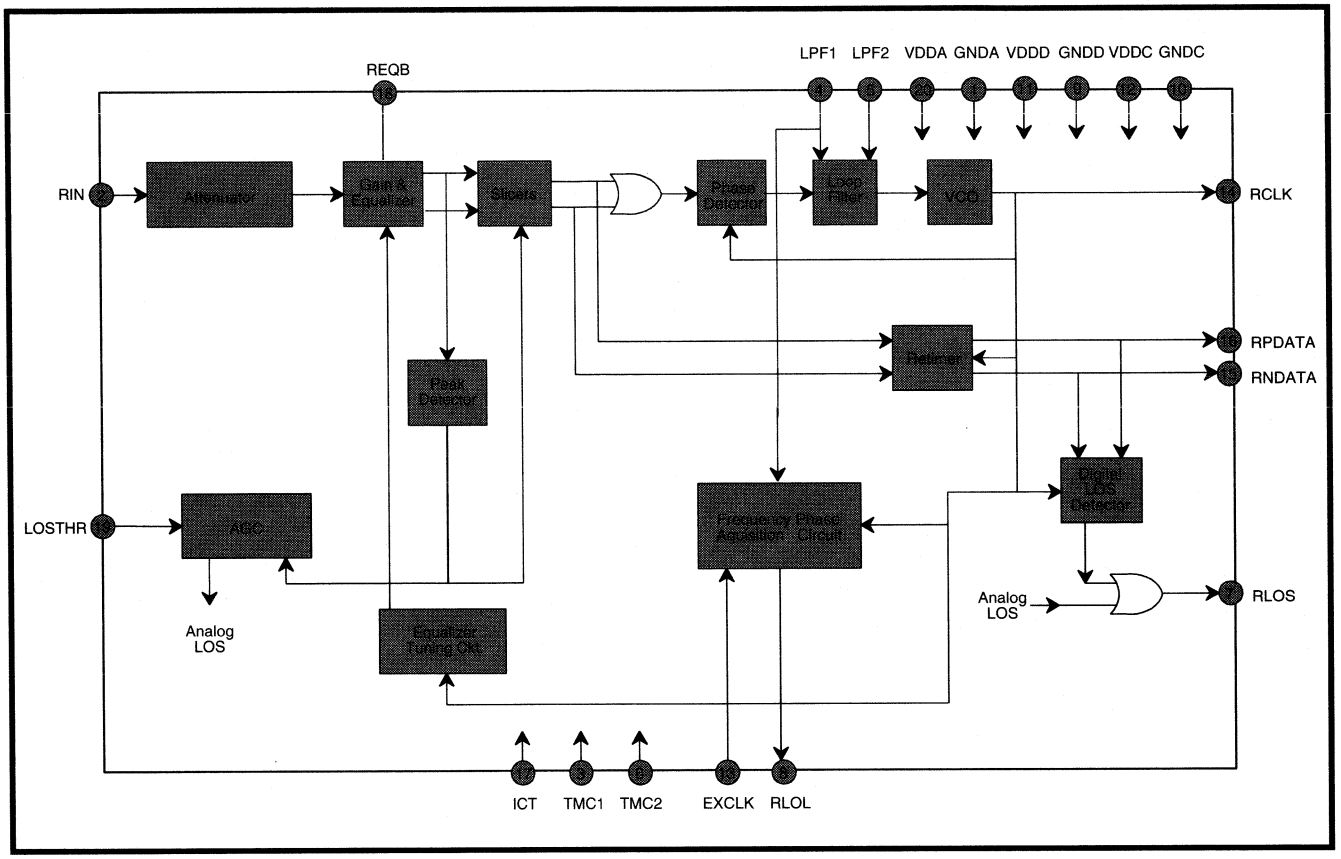
APPLICATIONS

- Interface to E3 Networks
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals
- Multiplexers

ORDERING INFORMATION

Operating Part No.	Package	Temperature Range
XRT7295-1EIP	20-Lead 300 Mil PDIP	-40°C to +85°C°
XRT7295-1EIW	20 J-Lead 300 Mil JEDEC SOJ	-40°C to +85°C

XRT7295E BLOCK DIAGRAM



DS3/STS-1/E3 INTEGRATED LINE TRANSMITTER

REV. 2.04

GENERAL DESCRIPTION

The XRT7296 is a fully integrated PCM Line Driver IC intended for DS3 (44.736Mbps) or E3 (34.368Mbps) applications. It can also be used for transmitting SONET STS-1 (51.84Mbps) signals over coaxial cable. The IC is designed to complement either XRT7295 DS3/SONET STS-1 or XRT7295E E3 Integrated Line Receivers. The XRT7296 converts input clock and dual-rail unipolar data into AMI pulses according to AT&T Technical Advisory No. 34 or CCITT G.703 recommendations.

The device provides B3ZS (DS3) or HDB3 (E3) encoding functions for data to be transmitted to the line. A complimentary decoder circuit is also included in the chip for decoding received signals from an external line receiver. Both encoder and decoder functions can be disabled independently through external control pins. In the receive direction, coding errors and bipolar violations are detected and flagged at an output pin.

On-chip pulse shaper circuitry eliminates normally required external components for line equalization to meet the cross-connect template. For system level trouble-shooting and testing, both local and remote loop-backs are possible with the built-in loop-back circuit.

The XRT7296 is manufactured using BiCMOS technology and is packaged in a 28-pin PDIP or SOJ packages. The device requires a single 5V power supply and consumes a maximum power of 700mW. (Line current feed + device dissipation).

FEATURES

- Fully Integrated Transmit Interface for DS3/STS-1 or E3
- Integrated Pulse Shaping Circuit
- Compliance with Compatibility Bulletin 119
- Compliance with CCITT Recommendations G.703 & G.824
- Compliance with Bellcore TR-NWT-000499
- Compliance with ANSI T1.404
- Built-in B3ZS/HDB3 Encoder and Decoder
- Remote and Local Loopback Functions
- Single 5V Power Supply

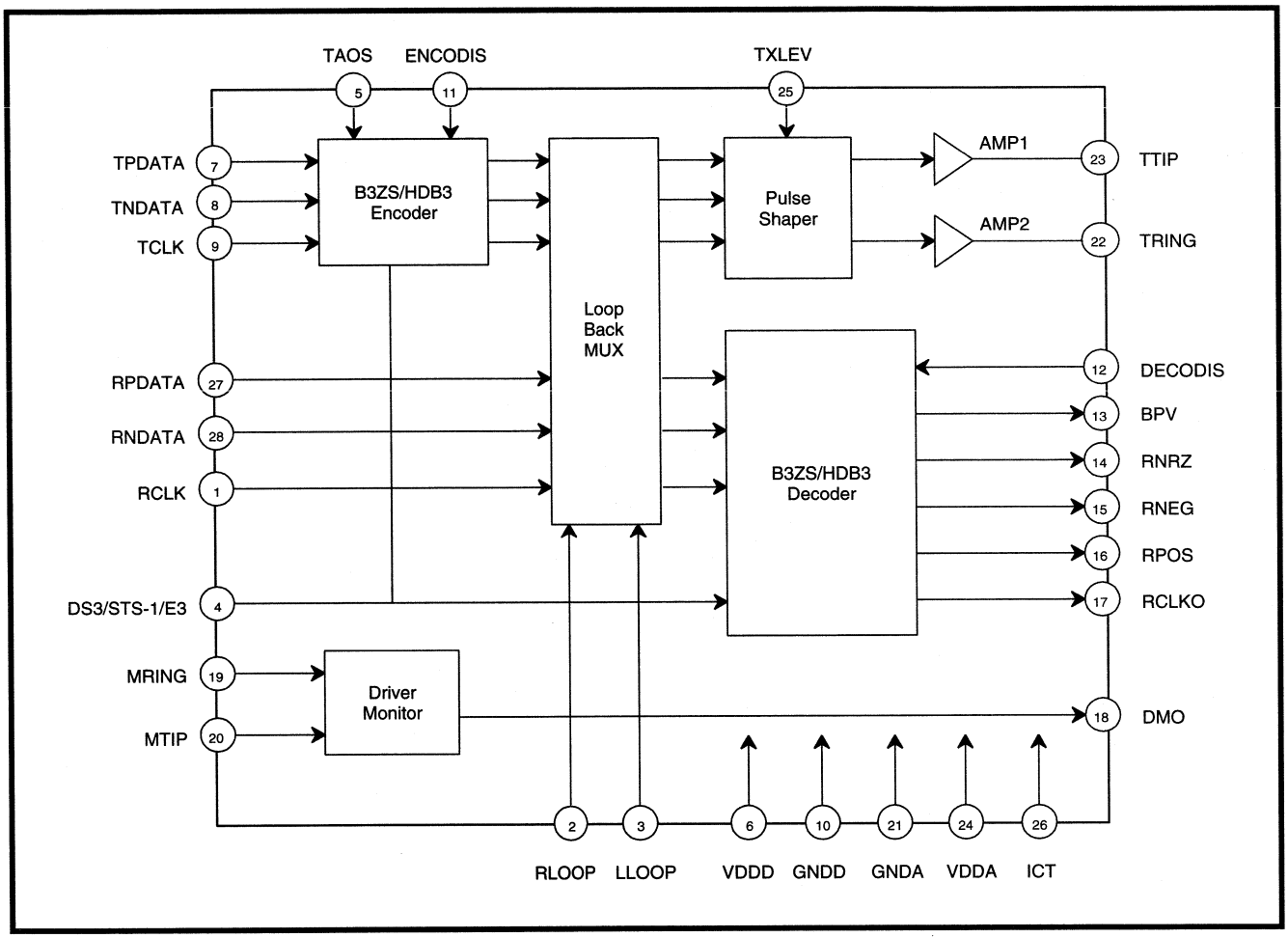
APPLICATIONS

- Interface for SONET, DS-3 and E3 Network Equipment
- Digital Cross-Connect Systems
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT7296IP	28-Lead 600 Mil PDIP	-40°C to +85°C
XRT7296IW	28 J-Lead 300 Mil JEDEC SOJ	-40°C to +85°C

XRT7296 BLOCK DIAGRAM



DS3/STS-1/E3 INTEGRATED LINE TRANSMITTER

GENERAL DESCRIPTION

The XRT7298 is a fully integrated PCM Line Driver IC intended for DS3 (44.736Mbps) or E3 (34.368Mbps) applications. It can also be used for transmitting SONET STS-1 (51.84Mbps) signals over coaxial cable. The IC is designed to complement either XRT7295 DS3/SONET STS-1 or XRT7295E E3 Integrated Line Receivers. The XRT7298 converts input clock and dual-rail unipolar data into AMI pulses according to AT&T Technical Advisory No. 34 or CCITT G.703 recommendations.

The device provides B3ZS (DS3) or HDB3 (E3) encoding functions for data to be transmitted to the line. A complimentary decoder circuit is also included in the chip for decoding received signals from an external line receiver. Both encoder and decoder functions can be disabled independently through external control pins. In the receive direction, coding errors and bipolar violations are detected and flagged at an output pin.

On-chip pulse shaper circuitry eliminates normally required external components for line equalization to meet the cross-connect template. For system level trouble-shooting and testing, both local and remote loop-backs are possible with the built-in loop-back circuit.

The XRT7298 device contains an "on-chip" Transmit Clock Duty Cycle Correction circuit. This circuit guarantees that the XRT7298 device will generate pulses, that will meet the various "pulse-template" requirements (e.g., ITU-T G.703 for E3, ANSI T1.404 and Bellcore TR-NWT-000499 for DS3); provided the user supplies a "transmit clock" signal, to the TCLK input pin (pin 9); that has duty cycle ranging from 30% to 70%. This feature eliminates the need for the user to provide a transmit clock signal (to TCLK), with a duty cycle ranging from 47% to 53% (for E3) and 45% to 55% (for DS3).

The XRT7298 is manufactured using BiCMOS technology and is packaged in a 28-pin PDIP or SOJ packages. The device requires a single 5V power supply and consumes a maximum power of 700mW. (Line current feed + device dissipation).

FEATURES

- Fully Integrated Transmit Interface for DS3/STS-1 or E3
- Integrated Pulse Shaping Circuit
- Compliance with Compatibility Bulletin 119
- Compliance with CCITT Recommendations G.703 & G.824
- Compliance with Bellcore TR-NWT-000499
- Compliance with ANSI T1.404
- Built-in B3ZS/HDB3 Encoder and Decoder
- Remote and Local Loopback Functions
- Single 5V Power Supply
- Contains Transmit Clock Duty Cycle Correction Circuit on Chip

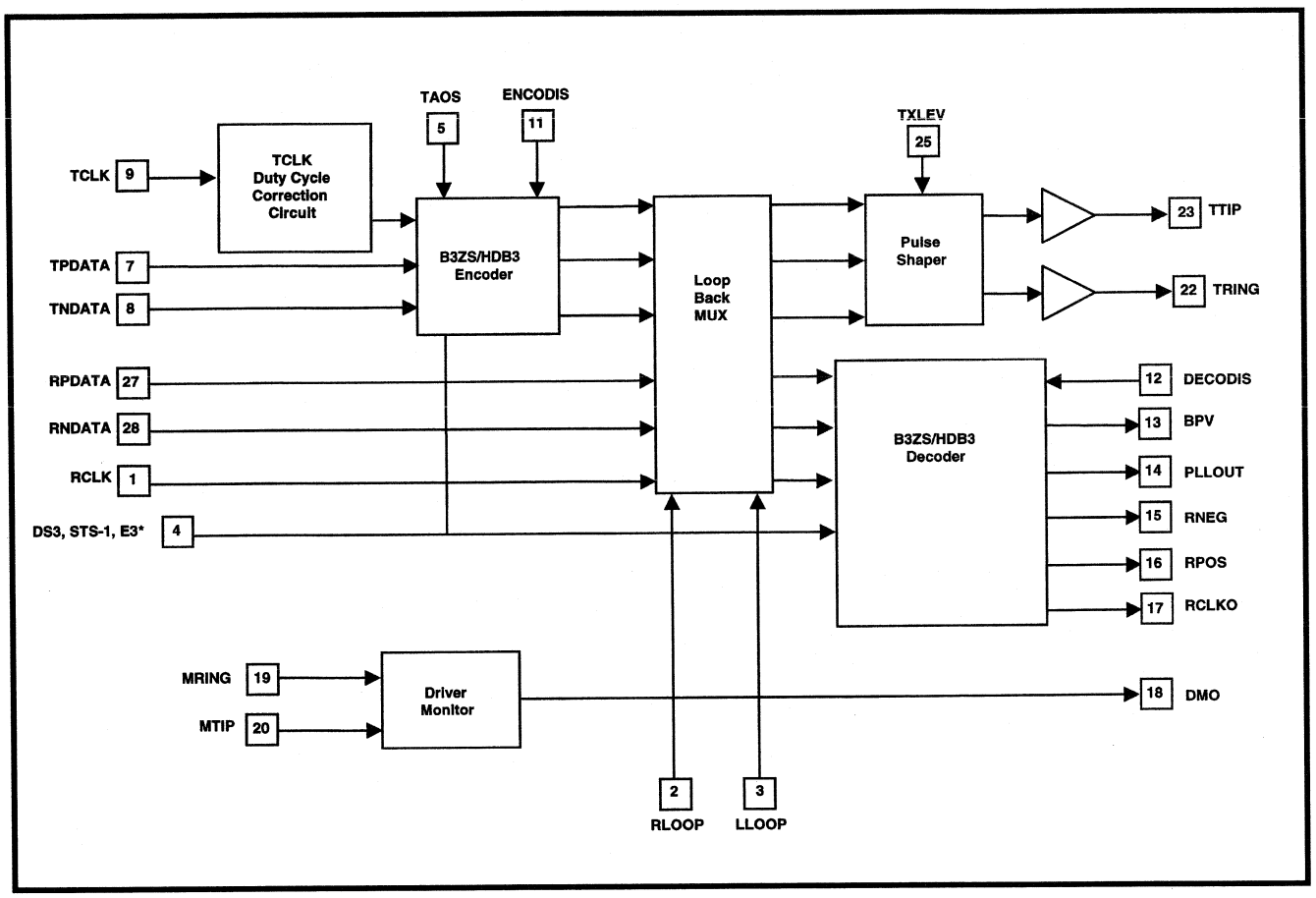
APPLICATIONS

- Interface for SONET, DS3 and E3 Network Equipment
- Digital Cross-Connect Systems
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT7298IP	28-Lead 600 Mil PDIP	-40° C to +85° C
XRT7298IW	28 J-Lead 300 Mil JEDEC SOJ	-40° C to +85° C

XRT7298 BLOCK DIAGRAM



DS3/E3/STS-1 LINE INTERFACE UNIT

GENERAL DESCRIPTION

The XRT7300 DS3/E3/STS-1 Line Interface Unit is designed to be used in DS3, E3 or SONET STS-1 applications and consists of a line transmitter and receiver integrated on a single chip.

XRT7300 can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates.

In the transmit direction, the XRT7300 encodes input data to either B3ZS (for DS3/STS-1 applications) or HDB3 (for E3 applications) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction the XRT7300 performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of line code violations.

The XRT7300 also contains a 4-Wire Microprocessor Serial Interface for accessing the on-chip Command registers.

FEATURES

- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Contains a 4-Wire Microprocessor Serial Interface
- Uses Minimum External components
- Requires Single +5V Power Supply
- -40°C to +85°C Operating Temperature Range
- Available in a 44 pin TQFP package

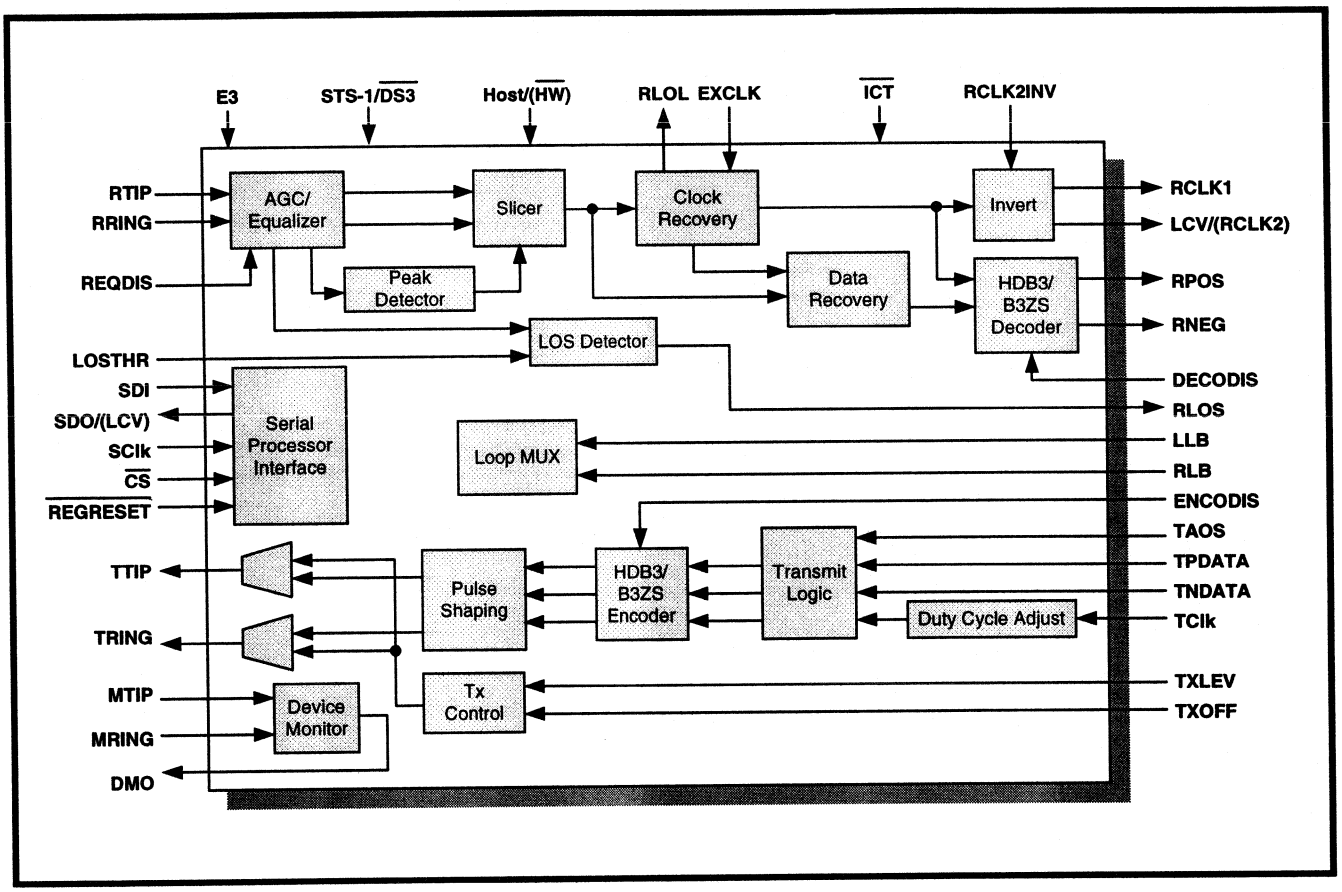
APPLICATIONS

- Interfaces to E3, DS3 or SONET STS-1 Networks
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals
- Multiplexers

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT7300IV	44-Lead TQFP (10 x 10mm)	-40°C to +85°C

XRT7300 BLOCK DIAGRAM



DS3/E3/STS-1 LINE INTERFACE UNIT

GENERAL DESCRIPTION

The XRT73L00A DS3/E3/STS-1 Line Interface Unit is designed to be used in DS3, E3 or SONET STS-1 applications and consists of a line transmitter and receiver integrated on a single chip.

XRT73L00A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates.

In the transmit direction, the XRT73L00A encodes input data to either B3ZS (for DS3/STS-1 applications) or HDB3 (for E3 applications) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction the XRT73L00A performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of line code violations.

The XRT73L00A also contains a 4-Wire Microprocessor Serial Interface for accessing the on-chip Command registers.

FEATURES

- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Contains a 4-Wire Microprocessor Serial Interface
- Uses Minimum External components
- Single +3.3V Power Supply
- 5 V Tolerant pins
- -40°C to +85°C Operating Temperature Range
- Available in a 44 pin TQFP package

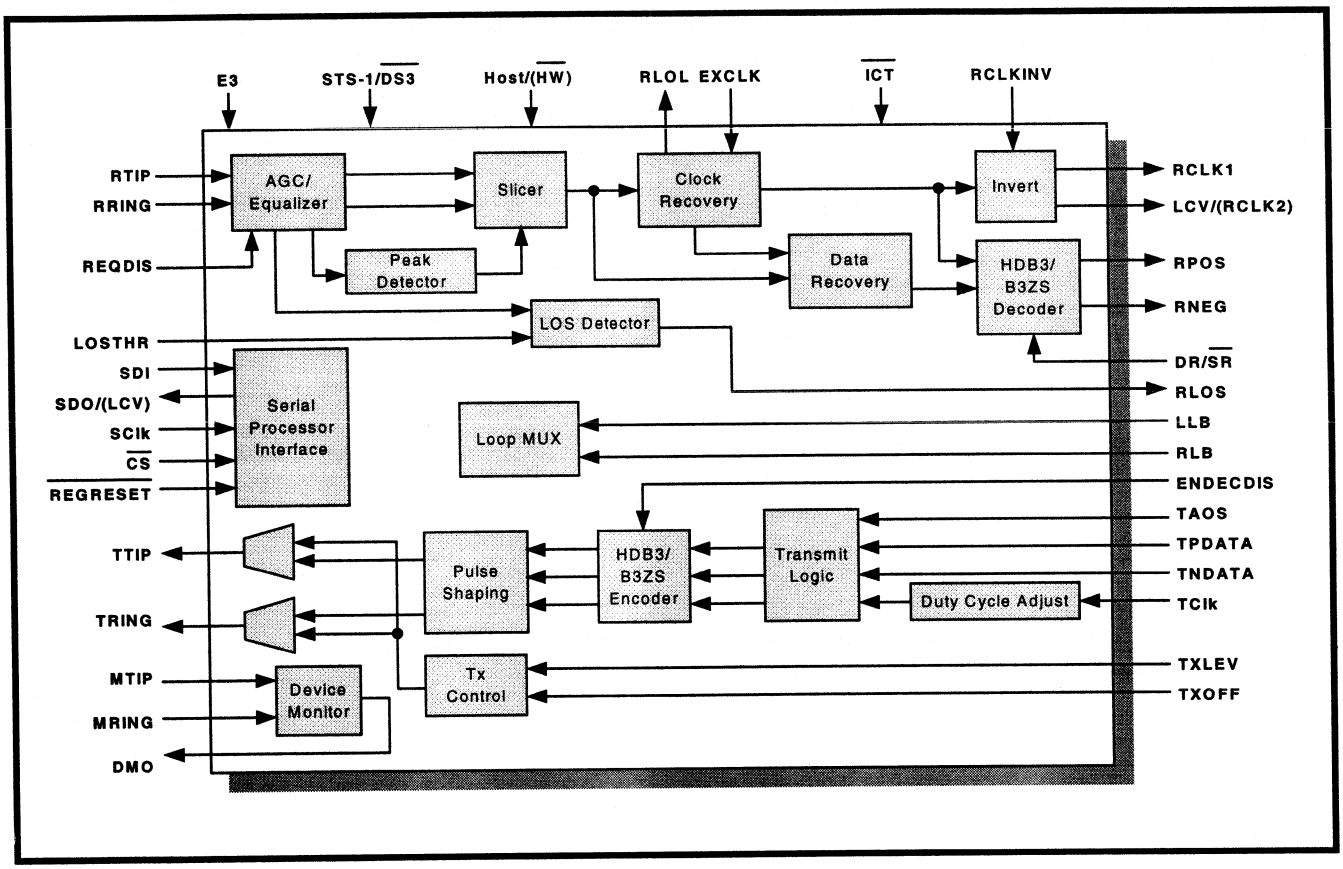
APPLICATIONS

- Interfaces to E3, DS3 or SONET STS-1 Networks
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals
- Multiplexers

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT73L00AIV	44-Lead TQFP (10 x 10mm)	-40°C to +85°C

XRT73L00A BLOCK DIAGRAM



TWO-CHANNEL DS3/E3/STS-1 LINE INTERFACE UNIT

REV. 1.1.6

GENERAL DESCRIPTION

The XRT7302 Dual Channel E3/DS3/STS-1 Transceiver IC consists of two fully integrated transmitter and receiver line transceivers designed for E3, DS3 or SONET STS-1 applications.

Each channel can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channel.

In the transmit direction, each channel in the XRT7302 encodes input data to either B3ZS or HDB3 format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT7302 can perform Equalization on incoming signals, perform Clock Recovery, decode data from either B3ZS or HDB3 format, convert the receive data into TTL/CMOS format, check for LOS or LOL conditions and detect and declare the occurrence of Line Code Violations.

FEATURES

- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Contains a 4-Wire Microprocessor Serial Interface
- Full Loop-back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Single +5V Power Supply
- Uses Minimum External components
- Operates over -40°C to +85°C Temperature Range
- Available in an 80 pin TQFP Thermal Enhanced package with integral Heat Sink

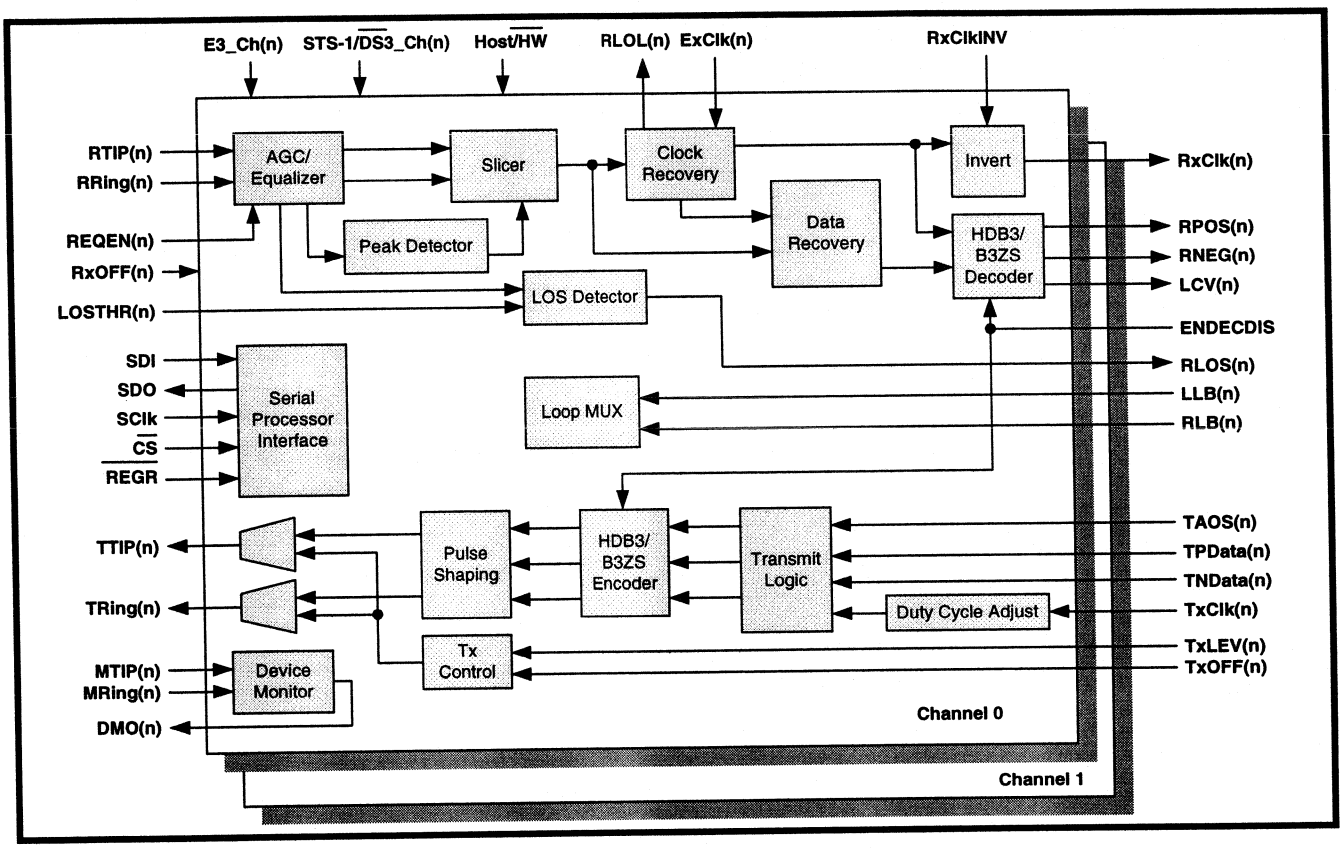
APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT7302IV	80-Lead TQFP	-40°C to +85°C

XRT7302 BLOCK DIAGRAM



NOTE: *1. (n) = 0 or 1 for the respective channel.*

2. Serial processor interface pins are shared by both channels in HOST Mode and are redefined in Hardware Mode

TWO-CHANNEL DS3/E3/STS-1 LINE INTERFACE UNIT

GENERAL DESCRIPTION

The XRT73L02A Dual Channel E3/DS3/STS-1 Transceiver IC consists of two fully integrated transmitter and receiver line transceivers designed for E3, DS3 or SONET STS-1 applications.

Each channel can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channel.

In the transmit direction, each channel in the XRT73L02A encodes input data to either B3ZS or HDB3 format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT73L02A can perform Equalization on incoming signals, perform Clock Recovery, decode data from either B3ZS or HDB3 format, convert the receive data into TTL/CMOS format, check for LOS or LOL conditions and detect and declare the occurrence of Line Code Violations.

FEATURES

- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Contains a 4-Wire Microprocessor Serial Interface
- Full Loop-back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Single +3.3V Power Supply
- Uses Minimum External components
- Operates over -40°C to +85°C Temperature Range
- Available in an 80 pin TQFP package
- Thermal Information
  - Theta JA = 23° C/W
  - Theta JC = 5.32° C/W

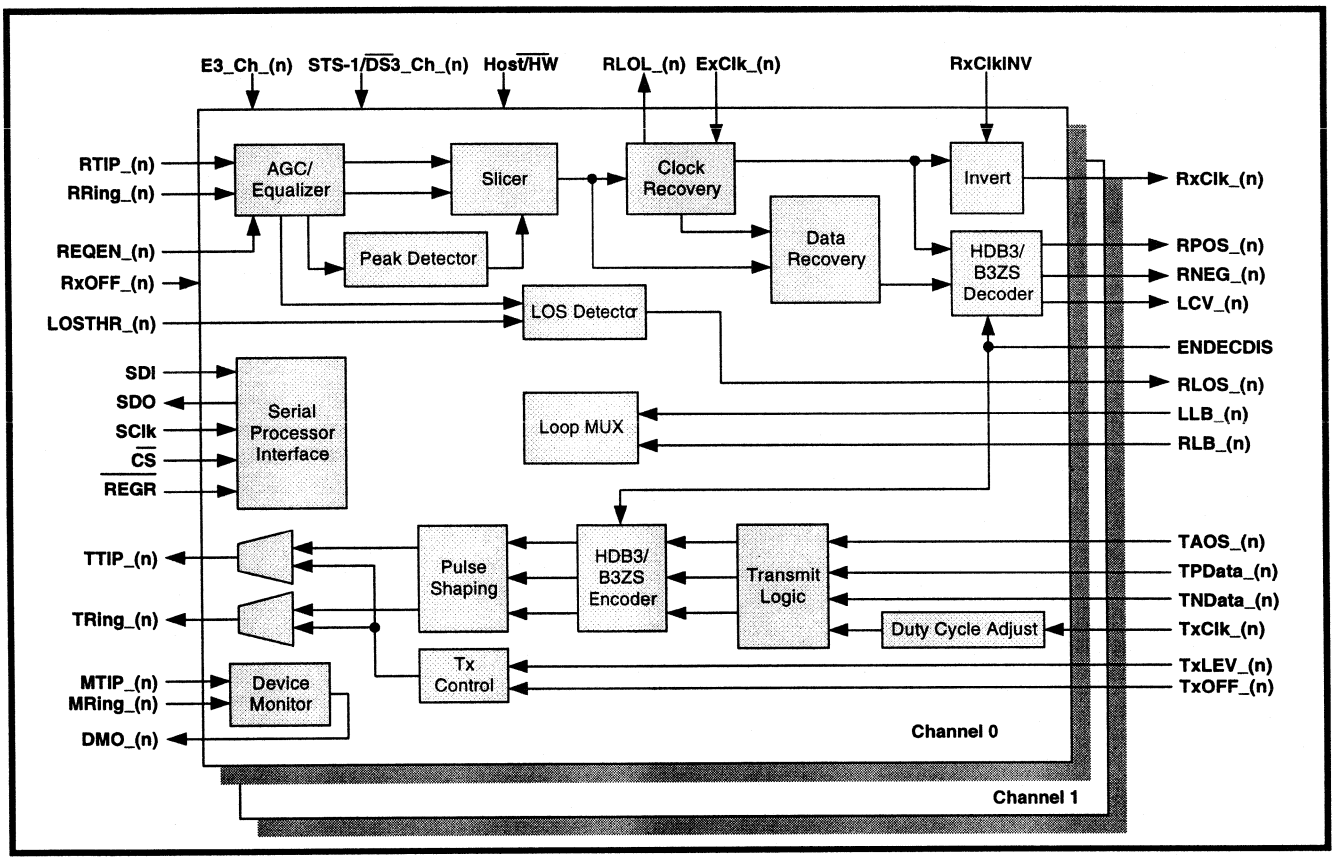
APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73L02AIV	80-Pin Thermally Enhanced TQFP	-40°C to +85°C

XRT73L02A BLOCK DIAGRAM



NOTE: *1. (n) = 0 or 1 for the respective channel.*

2. Serial processor interface pins are shared by both channels in HOST Mode and are redefined in Hardware Mode

THREE-CHANNEL DS3/E3/STS-1 LINE INTERFACE UNIT

GENERAL DESCRIPTION

The XRT73L03A, 3-Channel, DS3/E3/STS-1 Line Interface Unit consists of three independent line transmitters and receivers integrated on a single chip designed for DS3, E3 or SONET STS-1 applications.

Each channel of the XRT73L03A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channels.

In the transmit direction, each channel encodes input data to either B3ZS (DS3/STS-1) or HDB3 (E3) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT73L03A performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of Line Code Violations.

FEATURES

- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Contains a 4-Wire Microprocessor Serial Interface
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Uses Minimum External components
- Single +3.3V Power Supply
- 5V tolerant I/O
- -40°C to +85°C Operating Temperature Range
- Available in a Thermally Enhanced 120-pin TQFP package

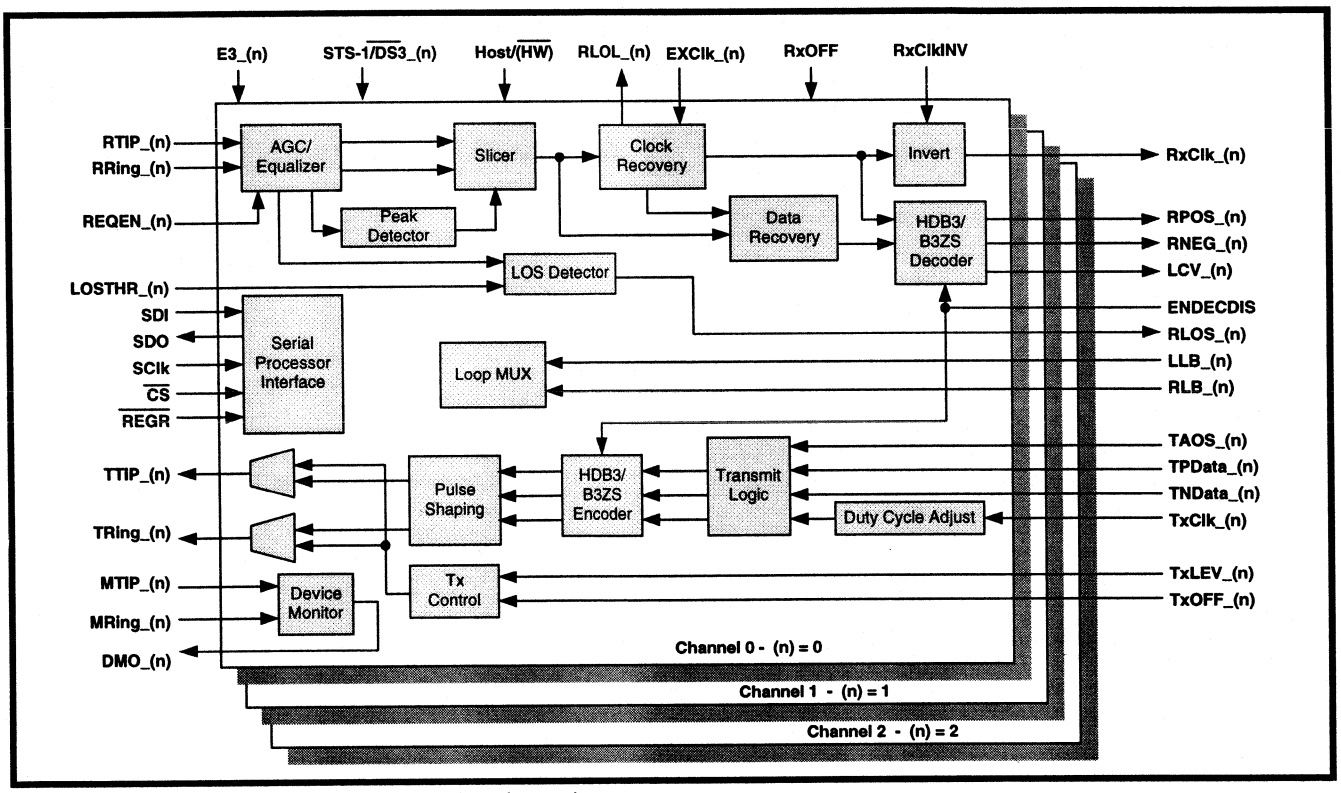
APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT73L03AIV	120-Lead TQFP (14 x 20 mm)	-40°C to +85°C

XRT73L03A BLOCK DIAGRAM



NOTE: *1. (n) = 0, 1, or 2 for the respective channels.*

2. Serial processor interface pins are shared by the three channels in HOST Mode and are redefined in Hardware Mode

FOUR-CHANNEL DS3/E3/STS-1 LINE INTERFACE UNIT

GENERAL DESCRIPTION

The XRT73L04A, 4-Channel, DS3/E3/STS-1 Line Interface Unit consists of four independent line transmitters and receivers integrated on a single chip designed for DS3, E3 or SONET STS-1 applications.

Each channel of the XRT73L04A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channels.

In the transmit direction, each channel encodes input data to either B3ZS (DS3/STS-1) or HDB3 (E3) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT73L04A performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of Line Code Violations.

FEATURES

- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Contains a 4-Wire Microprocessor Serial Interface
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Uses Minimum External components
- Single +3.3V Power Supply
- 5V tolerant I/O
- -40°C to +85°C Operating Temperature Range
- Available in a Thermally Enhanced 144 pin TQFP package
- Thermal Information
  - Theta JA = 20° C/W
  - Theta JC = 6° C/W

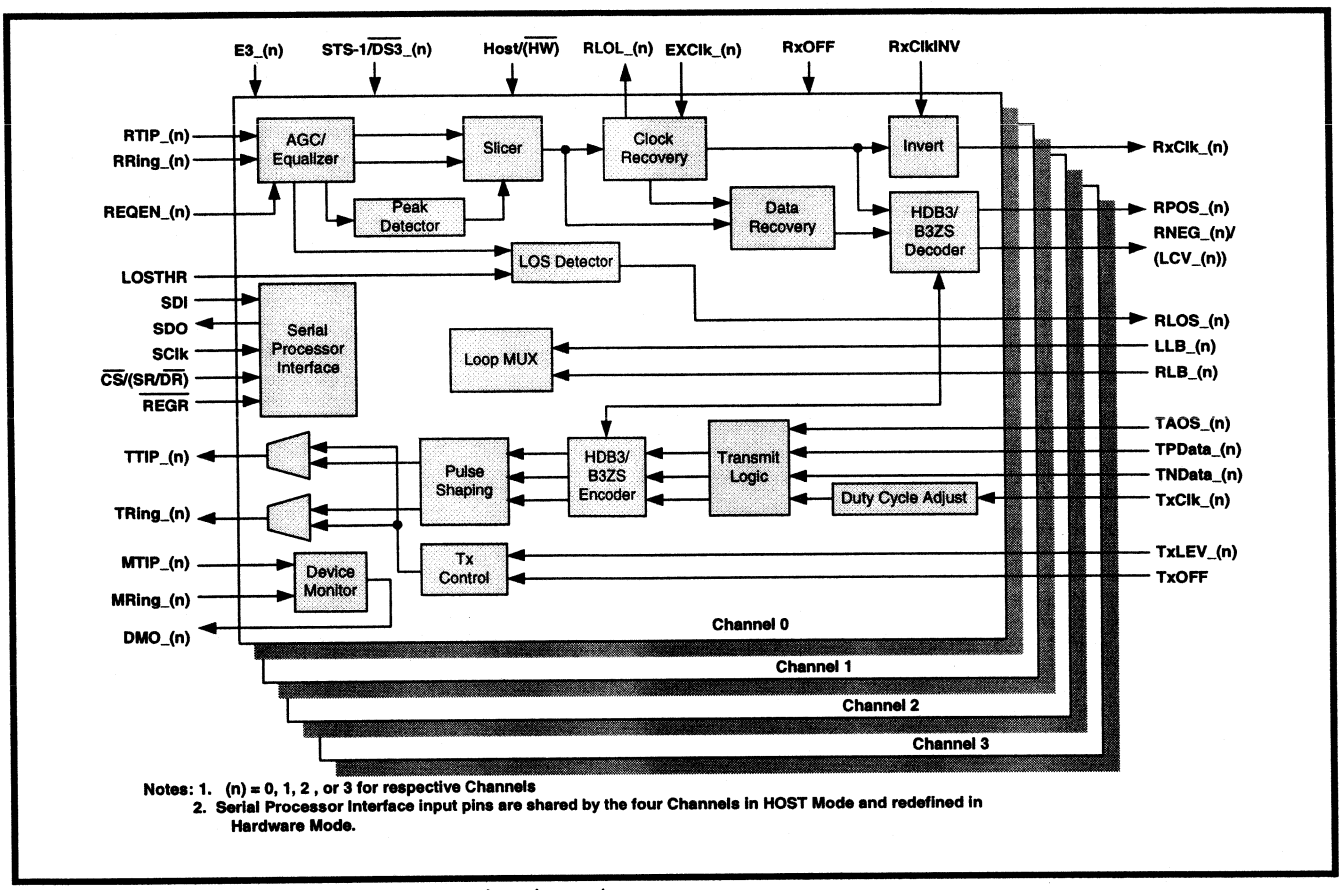
APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT73L04AIV	144-Lead TQFP (20 x 20 x 1.4 mm)	-40°C to +85°C

XRT73L04A BLOCK DIAGRAM



Notes: 1. (n) = 0, 1, 2 , or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the four Channels in HOST Mode and redefined in Hardware Mode.

NOTE: *1. (n) = 0, 1, 2, or 3 for the respective channels.*

2. Serial processor interface pins are shared by the four channels in HOST Mode and are redefined in Hardware Mode

THREE CHANNEL ATM UNI/PPP PHYSICAL LAYER PROCESSOR

GENERAL DESCRIPTION

The XRT74L73 3-Channel, ATM UNI/PPP Physical Layer Processor with integrated DS3/E3 framing controller is designed to support ATM direct mapping and cell delineation as well as PPP mapping and Frame processing. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3/E3 rates. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT74L73 DS3 ATM UNI/Clear-Channel Framer incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive functional sections.

FEATURES

- Compliant with 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface Specifications and supports UTOPIA Bus operating at 25, 33 or 50 MHz
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54-byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports ATM cell or PPP Packet Mapping
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8-Bit wide Intel, Motorola, PowerPC, and MIPS µPs
- HDLC controller per channel for Tx and Rx
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 388-ball PBGA Package

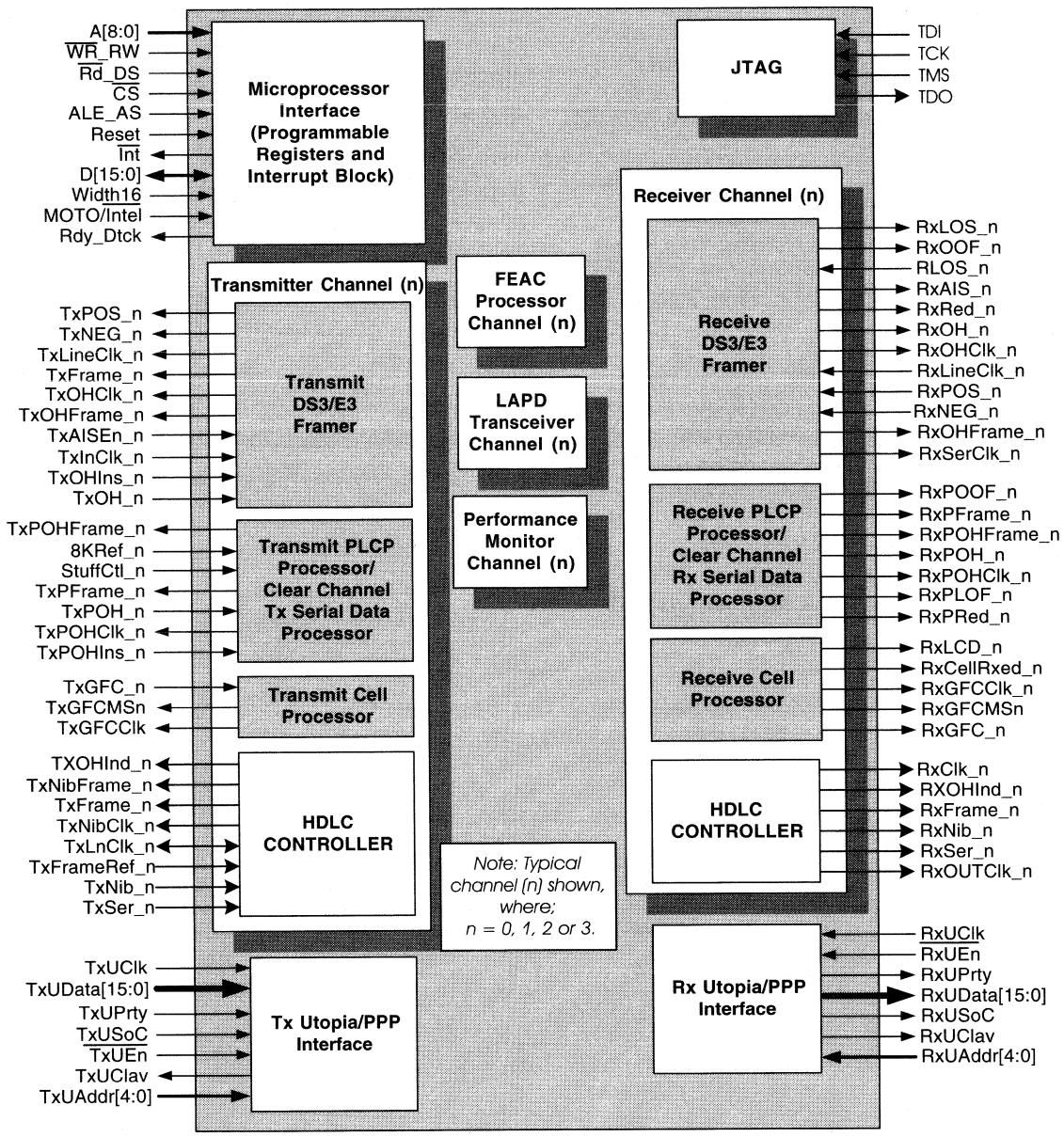
APPLICATIONS

- Digital Access and Cross Connect Systems
- Digital, ATM, WAN and LAN Switches
- Network Interface Service Units

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT74L73IB	388-Ball PBGA (35 x 35 mm)	-40°C to +85°C

XRT74L73 BLOCK DIAGRAM



FOUR CHANNEL ATM UNI/PPP PHYSICAL LAYER PROCESSOR

GENERAL DESCRIPTION

The XRT74L74 4-Channel, ATM UNI/PPP Physical Layer Processor with integrated DS3/E3 framing controller is designed to support ATM direct mapping and cell delineation as well as PPP mapping and Frame processing. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3/E3 rates. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT74L74 DS3 ATM UNI/Clear-Channel Framer incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive functional sections.

FEATURES

- Compliant with 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface Specifications and supports UTOPIA Bus operating at 25, 33 or 50 MHz
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports ATM cell or PPP Packet Mapping
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola, PowerPC, and MIPS µPs
- HDLC controller per channel for Tx and Rx
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 388-ball PBGA Package

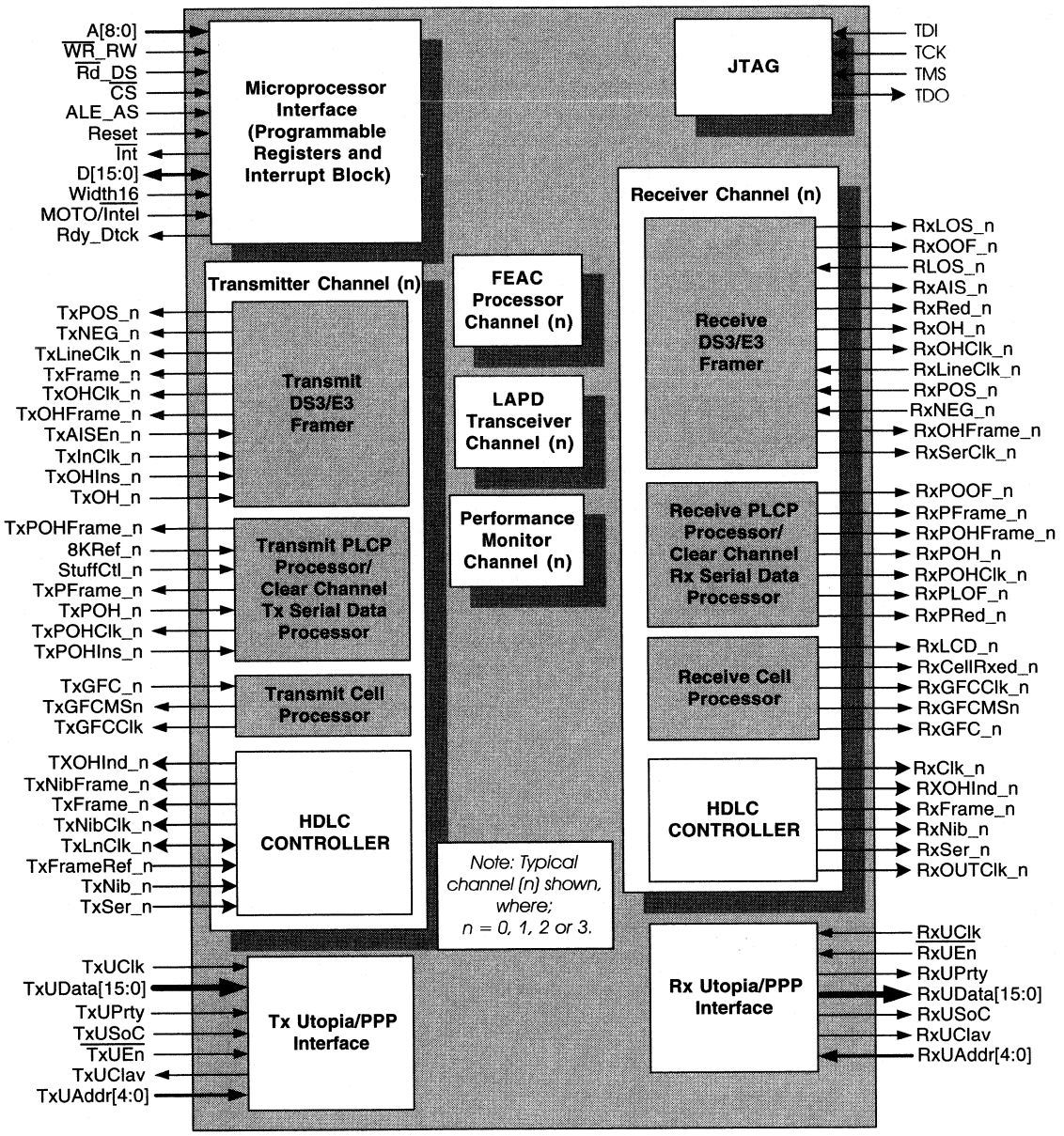
APPLICATIONS

- Digital Access and Cross Connect Systems
- Digital, ATM, WAN and LAN Switches
- Network Interface Service Units

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT74L74IB	388-Ball PBGA (35 x 35 mm)	-40°C to +85°C

XRT74L74 BLOCK DIAGRAM



THREE CHANNEL LINE INTERFACE UNIT WITH INTEGRATED JITTER ATTENUATOR

REV. P1.0.4

GENERAL DESCRIPTION

The XRT75L03 is a three-channel fully integrated line Interface Unit (LIU) with Jitter Attenuator for E3/DS3/ STS-1 applications. It incorporates 3 independent Receivers, Transmitters and Jitter Attenuators in a single 128 pin TQFP package.

Each channel of the XRT75L03 can be configured to operate in a mode/data rate, E3 (34.368 MHz),DS3 (44.736 MHz) or STS-1 (51.84 MHz) that is independent of each other.Each transmitter can be turned off or tri-stated for redundancy support and for conserving power.

The XRT75L03's differential receiver provides high noise interference margin and is able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.Depending on the cable length and for optimum performance, the receive equalizer can be either enabled or disabled.

The XRT75L03 incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications. Also, the Jitter Attenuator can be used for clock smoothing in SONET STS-1 to DS3 mapping.

The XRT75L03 provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The device supports local,remote and digital loop-backs and other diagnostic features that can be configured and controlled on a per-channel basis

FEATURES

RECEIVER:

- Integrated Adaptive Receive Equalizer.
- On chip Clock and Data Recovery circuit for high input jitter tolerance.
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements.
- Detects and Clears LOS as per G.775.
- Meets Bellcore GR-499 CORE Jitter Transfer Requirements.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation.
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards.
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled.

TRANSMITTER:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be turned on and off.

JITTER ATTENUATOR:

- On chip advanced crystal-less jitter attenuator for each channel.
- Jitter Attenuator can be selected in Receive or Transmit paths.
- Selectable FIFO size of 16 or 32 bits for Jitter Atten-uator.
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards.
- Jitter attenuator can be disabled.

CONTROL AND DIAGNOSTICS:

- 5 wire Serial Microprocessor Interface for control and configuration.
- Hardware Mode for control and configuration.
- Each channel supports Local, Remote and Digital Loop-backs.
- Single 3.3 V ± 5% power supply.
- 5 V Tolerant I/O.
- Available in 128 pin TQFP.
- -40°C to 85°C Industrial Temperature Range.

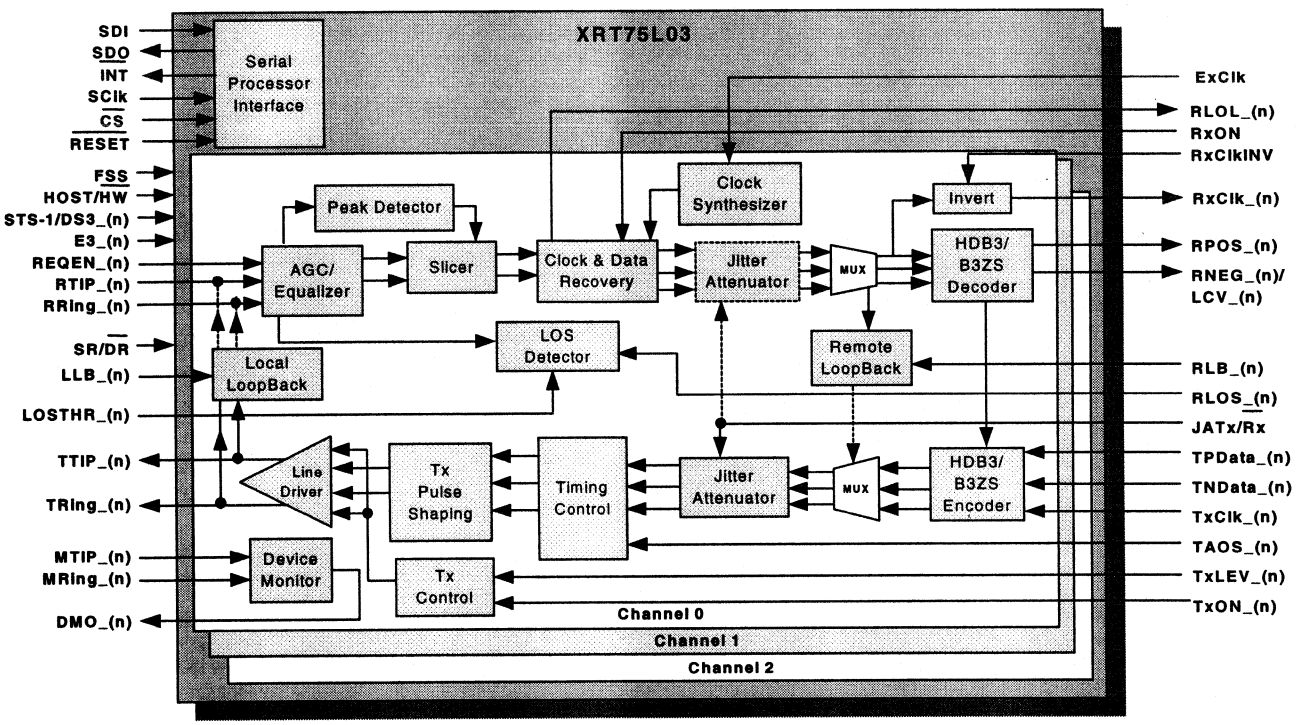
APPLICATIONS

- E3/DS3 Access Equipment.
- STS1-SPE to DS3 Mapper.
- DSLAMs.
- Digital Cross Connect Systems.
- CSU/DSU Equipment.
- Routers.
- Fiber Optic Terminals. Attenuator

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L03IV	128 Pin TQFP	-40°C to +85°C

XRT75L03 BLOCK DIAGRAM



NOTE: *1. (n) = 0, 1, or 2 for the respective channel.*

2. Serial processor interface pins are shared by the three channels in HOST Mode and are redefined in Hardware Mode

CLOCK SYNCHRONIZER/ADAPTER FOR COMMUNICATIONS

REV. 1.10

GENERAL DESCRIPTION

The XRT8000 is a dual phase-locked loop chip that generates two simultaneous, very low jitter, output clocks for synchronization applications in wide area networking systems. The outputs are phase locked to the input signal. The chip has four basic modes of operation; referred to as master (FORWARD, REVERSE) and slave (FORWARD, REVERSE) modes (See Figure 1). In the FORWARD mode it accepts up to 16th harmonic of either 1.544MHz or 2.048MHz as input reference and generates 1.2kHz and multiples of 2.4kHz, 56kHz or 64kHz. In the REVERSE mode an input clock of 56kHz or 64kHz is used to generate 1.544MHz or 2.048MHz output clocks. The SLAVE (FORWARD, REVERSE) modes generate the same output frequencies as the MASTER (FORWARD/ REVERSE MODES) except that the input frequency (FIN) is 8kHz. An optional divide by eight can be enabled at each of the outputs.

The input and output frequency selection can be done through a serial microprocessor interface. The XRT8000 is available in either 18 pin SOIC package or 18 pin plastic DIP.

FEATURES

- Clock Adaptation for Most Popular Telecommunication Frequencies
- Wide Input Frequency Range
- Programmable Output Frequencies
- Less than 0.05UI Wide Band Output Jitter
- Low Power Operation (5V and 3.3V)
- Maximum Lock Time of 45mS
- Cascadable
- No External Components Needed
- Lock Detect Indication Pin

APPLICATIONS

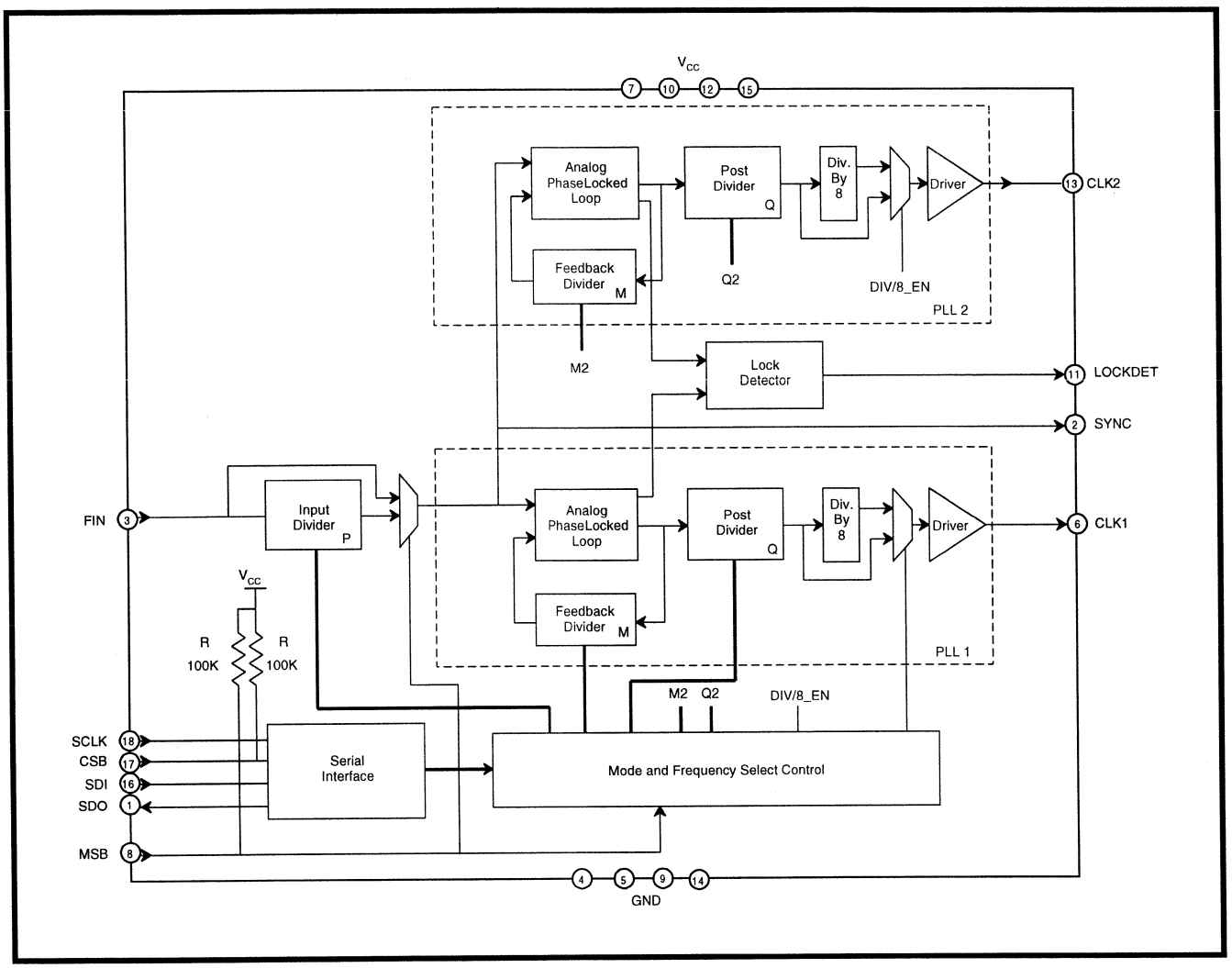
- DSU's, CSU's and Access Equipment
- ISDN Terminals
- Concentrators and Multiplexers

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT8000IP	18-Lead 300 Mil PDIP	-40°C to +85°C
XRT8000D	18-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

NOTE: Use XRT8001 for new designs

XRT8000 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT8001 WAN Clock is a dual-phase-locked loop chip that generates two very low jitter output clock signals that can be used for synchronization clocks in wide area networking systems. The XRT8001 has pre-programmed multipliers and dividers that are selected via the serial port. It generates two integer multiples of 8kHz, 56kHz, and 64kHz while locked onto an incoming reference of 1.54MHz (T1), 2.048MHz (E1), 8kHz, 56kHz, or 64kHz

The XRT8001 WAN Clock can be configured to operate in one of six modes:

1. The Forward/Master Mode
2. The Reverse/Master Mode
3. The "Fractional T1/E1" Reverse/Master Mode
4. The "E1 to T1 - Forward/Master" Mode
5. The "High Speed - Reverse" Mode
6. The "Slave" Mode

FEATURES

- Dual Phased Locked Loops with Pre-Programmed Multipliers and Dividers
- Pre-Programmed with Popular Frequency Conversions for Communications Systems
- Generates Output Clock Frequencies Ranging From 8kHz up to 16.384MHz
- Serial Port Control for Optimal Performance
- Sync Output: 8kHz or 64kHz
- Low Jitter
- Cascadable (Master / Slave Modes)
- No External Components Needed
- Pin Compatible with the XRT8000
- Low Power (3.3V or 5V): 40 - 100mW
- - 40°C to +85°C Temperature Range
- 18-Lead PDIP or SOIC Packages

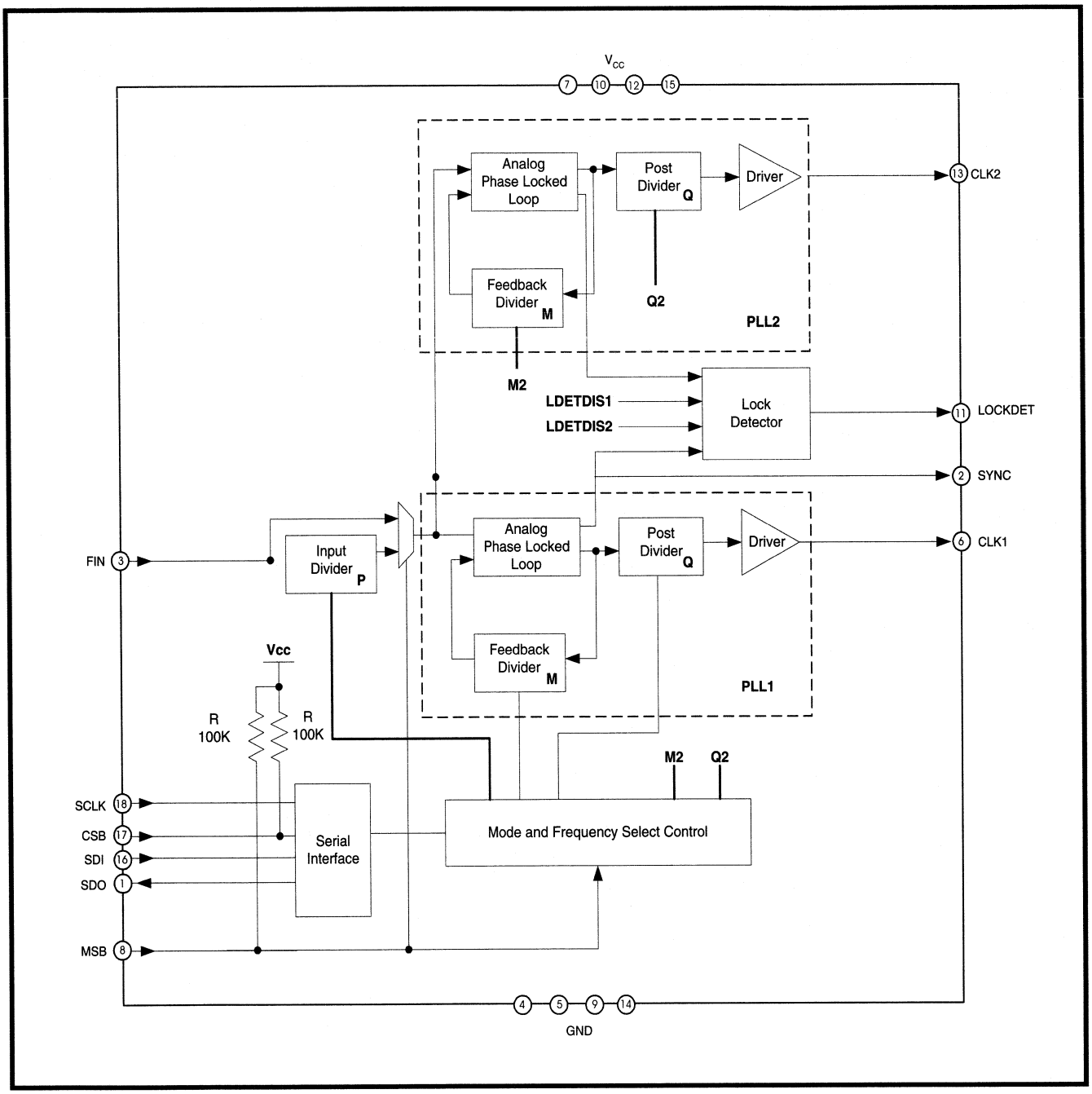
APPLICATIONS

- T1/E1 Access Equipment (DSU/CSU)
- Frame Relay Access Devices (FRAD)
- Basic Rate and Primary Rate ISDN Equipment
- ISDN Routers
- Terminals
- Remote Access Servers
- T1/E1 Concentrators
- T1/E1 Multiplexers
- T1/E1 Clock Rate Converters
- Internal Timing Generators
- System Synchronizers

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT8001IP	18-Lead 300 Mil PDIP	-40°C to +85°C
XRT8001ID	18-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

XRT8001 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT81L27 is an optimized seven-channel, analog, 3.3V, line interface unit, fabricated using low power CMOS technology. The device contains seven independent E1 channels, including data and clock recovery circuits. It is primarily targeted towards the SDH multiplexers that accomodate TU12 Tributary Unit Frames. Line cards in these units mutiplex 21 E1 channels into higher SDH rates. Devices with seven E1 interfaces such as the XRT81L27 provide the most efficient method of implementing 21-channel line cards. Each channel performs the driver and receiver functions necessary to convert bipolar signals to logical levels and vice versa.

The receiver input accepts transformer or capacitor coupled signals, while the transmitter is coupled to the line using a 1:2 step-up transformer. The same transformer configuration can be used for both balanced 120 Ω and unbalanced 75 Ω interfaces. The Receiver Loss of Signal Detection is compliant to G.775 and in Host Mode, the number of zeros received before LOS is declared can be increased to 4096 bits. This feature provides the user with the flexability to implement LOS specifications that require greater than G.775 requirements

FEATURES

- Consists of Seven (7) Independent E1 (CEPT) Line Interface Units (Transmitter and Receiver)
- Generates Transmit Output Pulses that are Compliant with the ITU-T G.703 Pulse Template Requirement for 2.048Mbps (E1) Rates
- On-Chip Pulse Shaping for both 75Ω and 120Ω line drivers
- Receiver Can Either Be Transformer or Capacitive-Coupled to the Line
- Detects and Clears LOS (Loss of Signal) Per ITU-T G.775
- Compliant with the ITU-T G.823 Jitter Tolerance Requirements

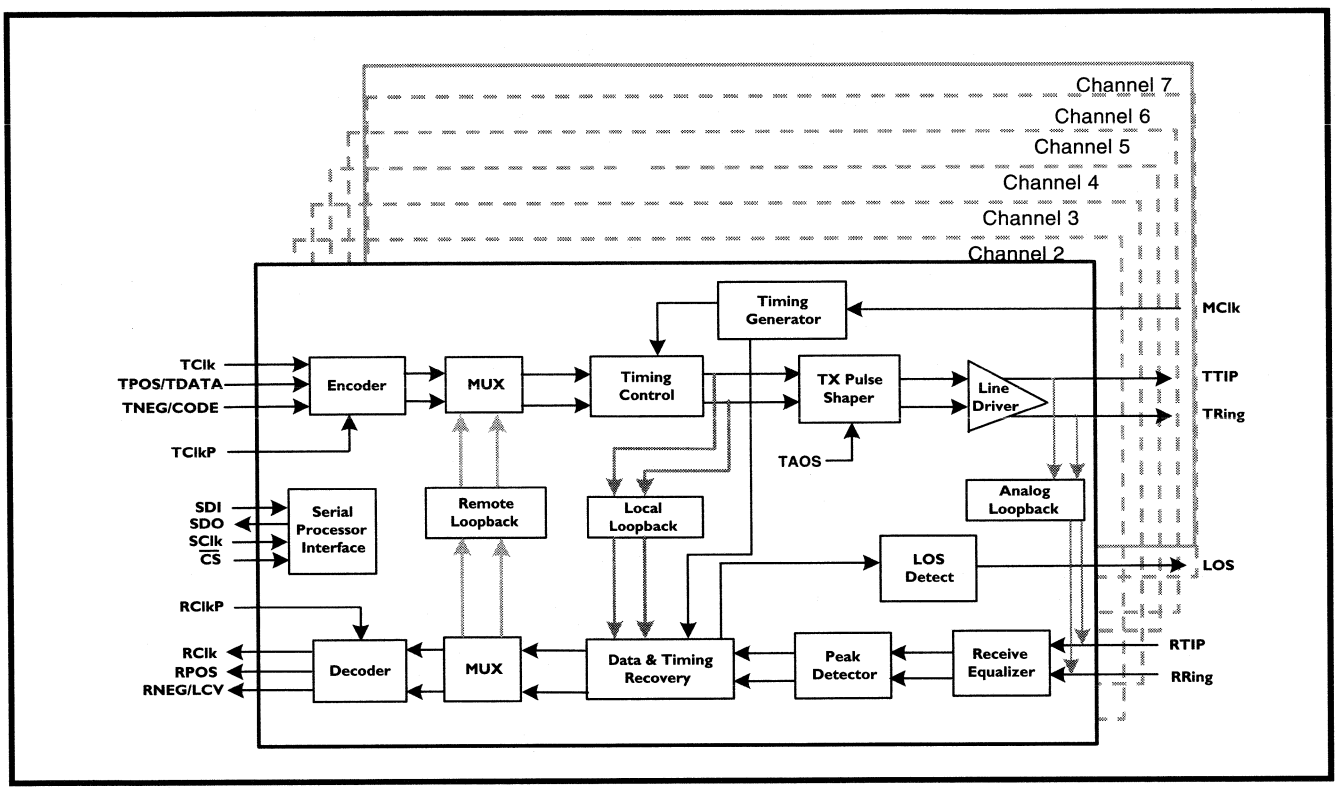
APPLICATIONS

- IPDH Multiplexers
- SDH Multiplexers
- Digital Cross-Connect Systems
- DECT (Digital European Cordless Telephone) Base Stations
- CSU/DSU Equipment

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT81L27IV	128-Lead TQFP	-40°C to +85°C

XRT81L27 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT82D20 is a fully integrated, single channel, Line Interface Unit (Transceiver) for 75 Ω or 120 Ω E1 (2.048 Mbps) applications. The LIU consists of a receiver with adaptive data slicer for accurate data and clock recovery and a transmitter which accepts either single or dual-rail digital inputs for signal transmission to the line using a low- impedance differential line driver. The LIU also includes a crystal-less jitter attenuator for clock and data smoothing which, depending on system requirements, can be selected in either the transmit or receive path.

Coupling the XRT82D20 to the line requires transformers on both the Receiver and Transmitter sides, and supports both 120 Ω balanced and 75 Ω unbalanced interfaces. The receiver can be capacitive coupled to for cost reduction

FEATURES

- Complete E1 (CEPT) line interface unit
- Generates transmit output pulses that are compliant with the ITU-T G.703 Pulse Template for 2.048Mbps (E1) rates
- On-Chip Pulse Shaping for both 75 Ω and 120 Ω Line Drivers
- Clock Recovery and Selectable Crystal-less Jitter attenuator
- Compliant with ETS300166 Return Loss
- Compliant with the ITU-T G.823 Jitter Tolerance Requirements
- Remote, Local and Digital Loop backs
- Declares and Clears LOS per ITU-T G.775
- Logic Inputs accept either 3.3V or 5.0V levels
- - 40^0C to 85^0C Temperature Range
- Low Power Dissipation; 145mW with 120 Ω or 160mW with 75 Ω typical
- +3.3V or +5V Supply Operation
- Pin Compatible with the XRT7288

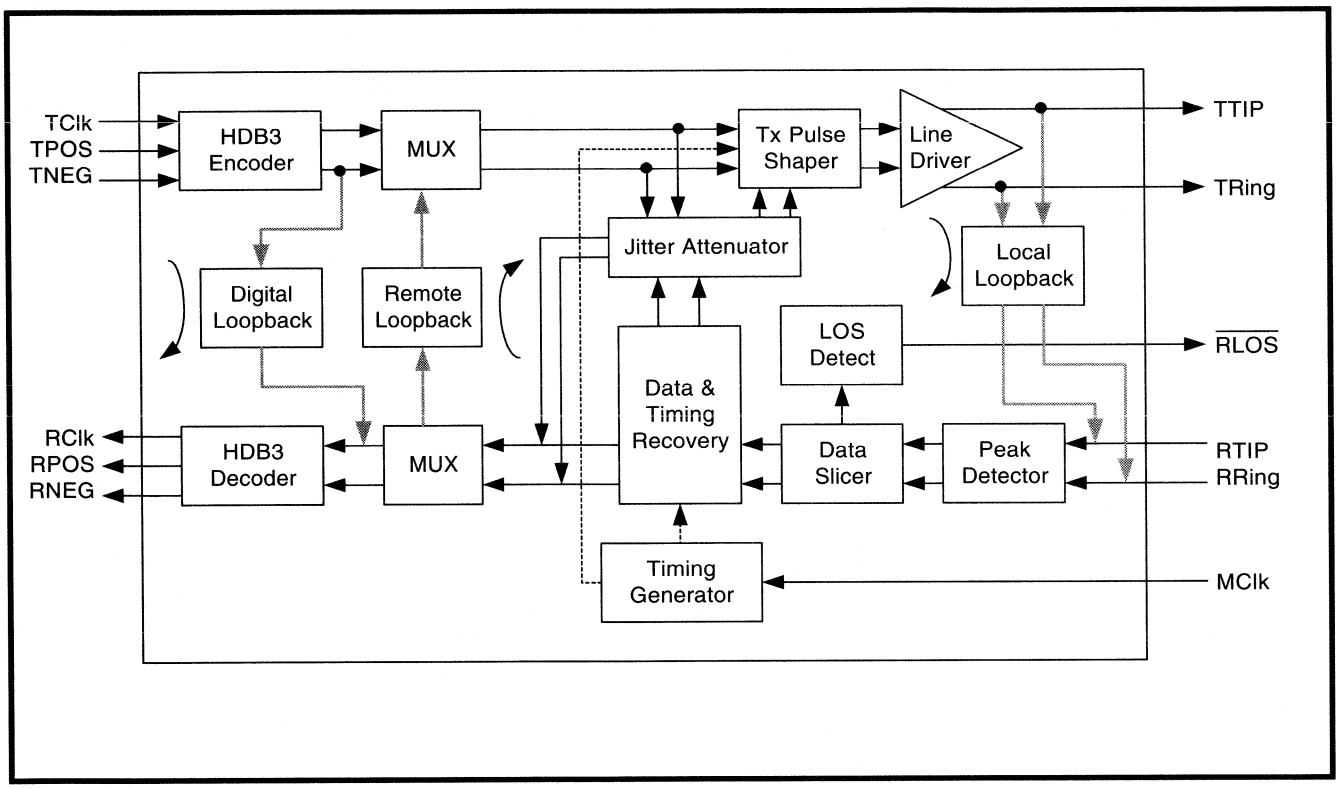
APPLICATIONS

- PDH Multiplexers
- SDH Multiplexers
- Digital Cross-Connect Systems
- DECT (Digital European Cordless Telephone) Base Stations
- CSU/DSU Equipment
- Test Equipment

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT82D20IW	28-Lead 300-Mil JEDEC SOJ	-40°C to + 85°C

XRT82D20 BLOCK DIAGRAM



FOUR-CHANNEL E1 LINE TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

REV. 1.1.0

GENERAL DESCRIPTION

The XRT82L24 is a fully integrated Quad (four channels) short-haul line interface unit for E1(2.048Mbps) 75Ω or 120Ω applications. Each channel consists of a receiver with equalizer for reliable data and clock recovery, and a transmitter which accepts either single or dual-rail digital inputs for signal transmission to the line using a low output impedance line driver. The device also includes a crystal-less jitter attenuator which, depending on system requirements, can be selected in the receive or transmit path through the Host or Hardware Mode control.

XRT82L24 is a low power CMOS device operating on a single 3.3V supply with 5V tolerant digital inputs.

FEATURES

- Fully integrated quad, short-haul PCM transceivers for E1 applications.
- On Chip Receive Equalizer and Transmit Pulse Shaper for CEPT 75Ω and 120Ω line terminations
- On chip clock recovery circuit
- Transformer or capacitor coupled receiver inputs
- Crystal-less jitter attenuator can be selected in the transmit or receive path
- High receiver interference immunity
- Per-channel transmit power shutdown
- Tri-state transmit output capability
- On chip per-channel driver failure monitoring circuit
- On chip HDB3/B8ZS/AMI encoder/decoder functions
- Transmit return loss meets or exceeds ETSI 300 166 standard
- Meets or exceeds specifications in ITU G.703, G.775, G.736 and G.823; ETSI 300-166
- 3.3V or 5.0V Logic level inputs
- Single +3.3V Supply Operation
- Same pin out as XRT82L34 T1/E1/J1 LIU

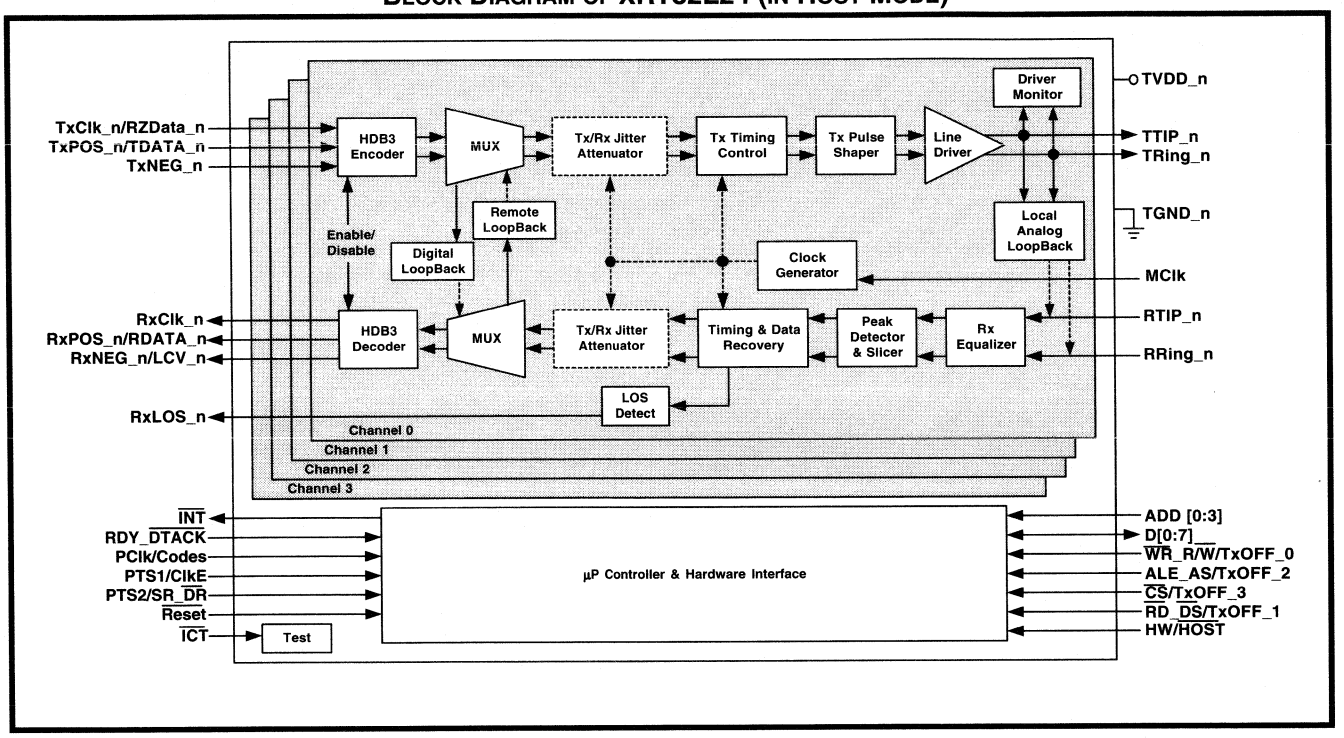
APPLICATIONS

- Digital cross connects (DSX-1)
- Channel Banks
- High speed data transmission line cards
- E1 Multiplexer
- Public switching systems and PBX interface

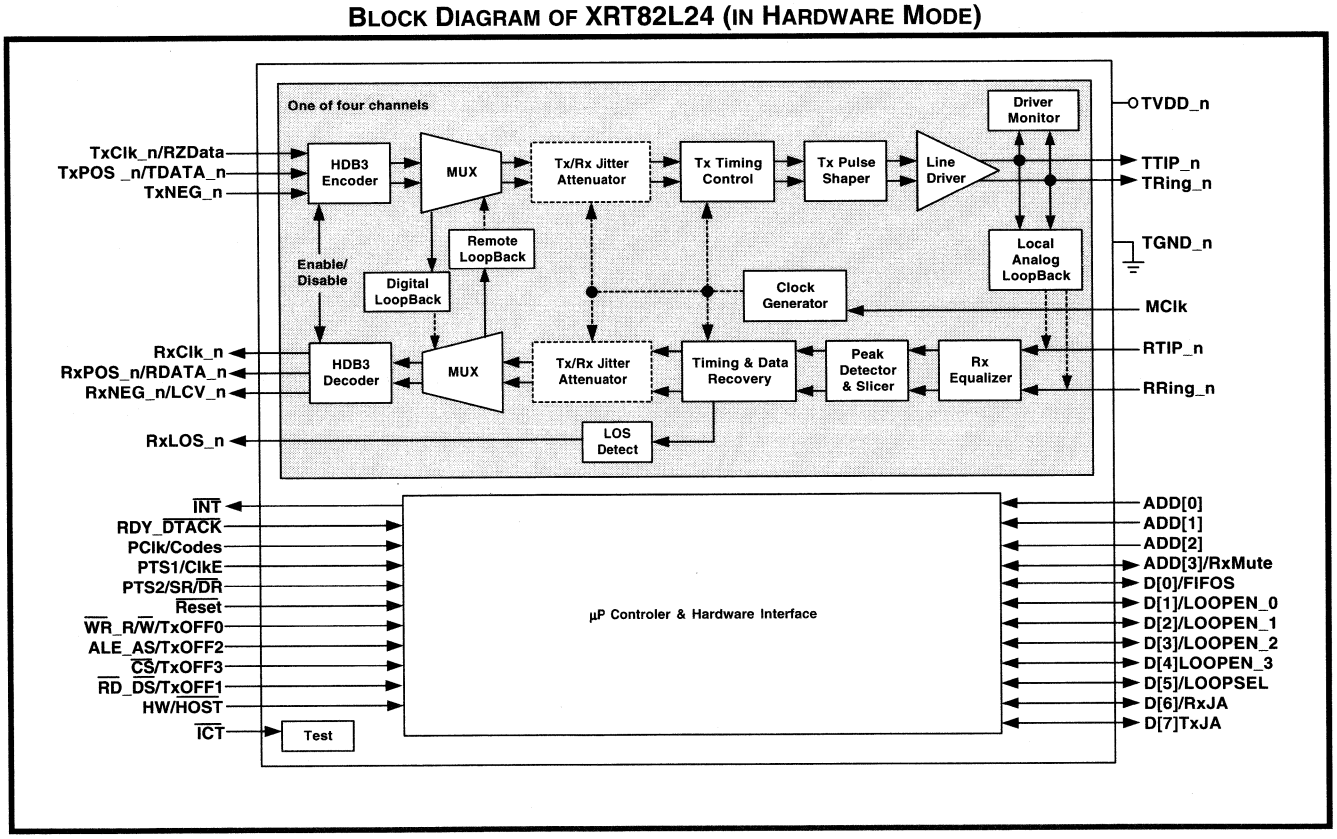
ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT82L24IV	100-Lead TQFP (14 x 14 x 1.4 mm)	-40°C to +85°C

BLOCK DIAGRAM OF XRT82L24 (IN HOST MODE)



BLOCK DIAGRAM OF XRT82L24 (IN HARDWARE MODE)



FOUR-CHANNEL T1/E1/J1 LINE TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

REV. 1.0.0

GENERAL DESCRIPTION

The XRT82L34 is a fully integrated Quad (four channels) short-haul line interface unit for T1(1.544Mbps) 100Ω and E1(2.048Mbps) 75Ω or 120Ω applications. Each channel consists of a receiver with equalizer for reliable data and clock recovery, and a transmitter which accepts either single or dual-rail digital inputs for signal transmission to the line using a low output impedance line driver. The device also includes a crystal-less jitter attenuator which, depending on system requirements, can be selected in the receive or transmit path through the Host or Hardware Mode control.

XRT82L34 is a low power CMOS device operating on a single 3.3V supply with 5V tolerant digital inputs.

FEATURES

- Fully integrated quad, short-haul PCM transceivers for E1 and T1 applications.
- On Chip Receive Equalizer and Transmit Pulse Shaper for DS1 Digital Cross Connect (DSX-1) and CEPT 75Ω and 120Ω line terminations
- On chip clock recovery circuit
- Transformer or capacitor coupled receiver inputs
- Crystal-less jitter attenuator can be selected in the transmit or receive path
- High receiver interference immunity
- Per-channel transmit power shutdown
- Tri-state transmit output capability
- On chip per-channel driver failure monitoring circuit
- On chip HDB3/B8ZS/AMI encoder/decoder functions
- Transmit return loss meets or exceeds ETSI 300 166 standard
- Meets or exceeds specifications in ITU G.703, G.775, G.736 and G.823; Bellcore GR-499-CORE; ANSI T1.403 and ETSI 300-166
- 3.3V or 5.0V Logic level inputs
- Single +3.3V Supply Operation

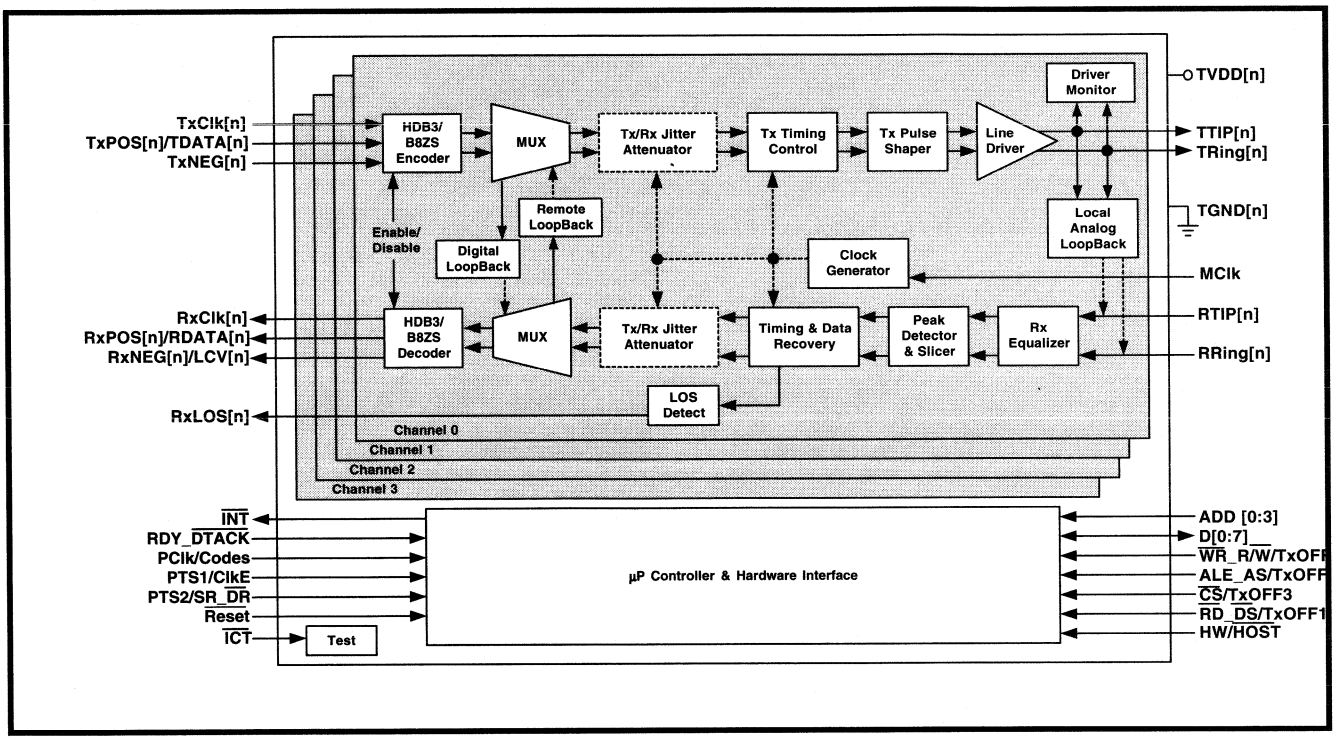
APPLICATIONS

- Digital cross connects (DSX-1)
- Channel Banks
- High speed data transmission line cards
- T1/E1 Multiplexer
- Public switching systems and PBX interfaces

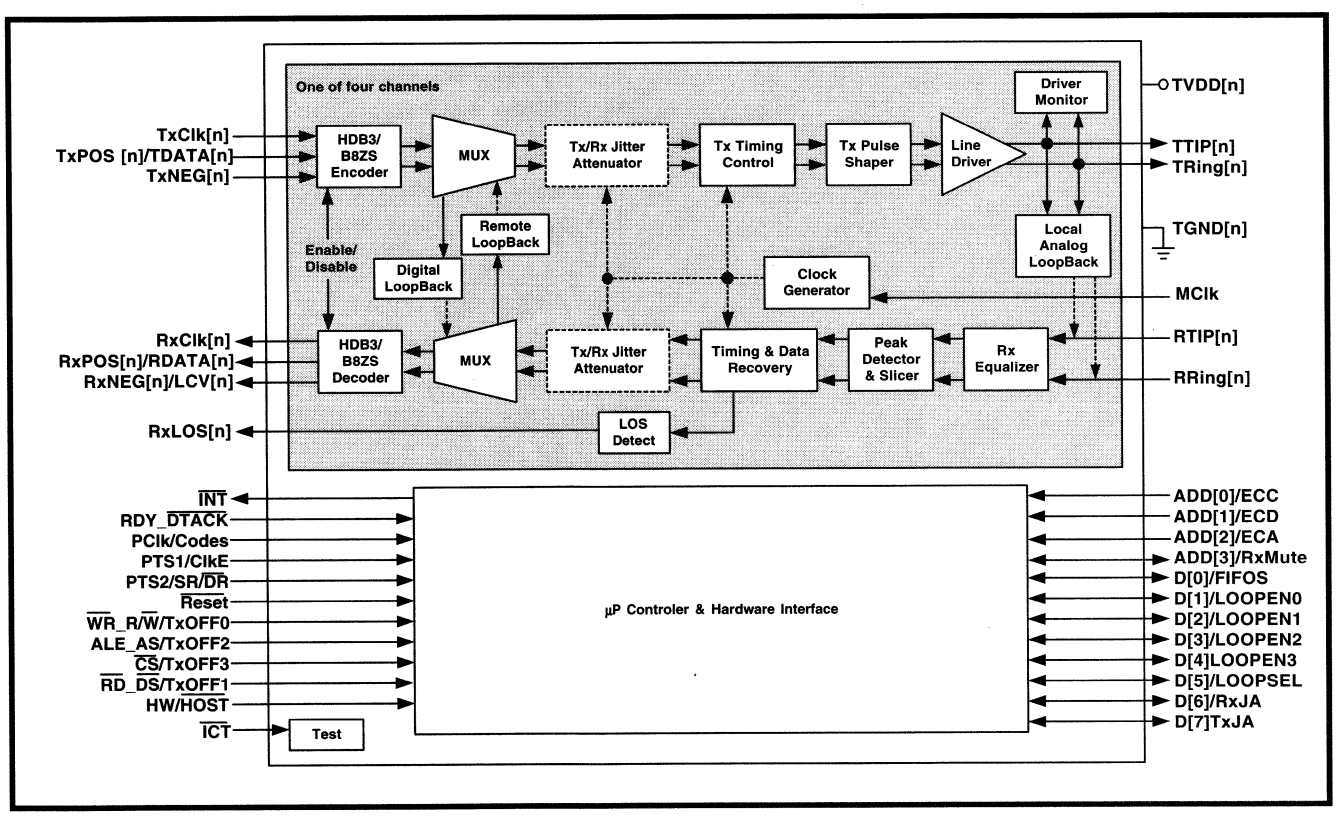
ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT82L34IV	100-Lead TQFP (14 x 14 x 1.4 mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT82L34 T1/E1/J1 LIU (HOST MODE)



BLOCK DIAGRAM OF THE XRT82L34 T1/E1/J1 LIU (HARDWARE MODE)



EIGHT-CHANNEL T1/E1/J1 LINE TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

GENERAL DESCRIPTION

XRT82L38 is a fully integrated octal (eight channels) short-haul line interface unit for T1(1.544Mbps) 100Ω and E1(2.048Mbps) 75Ω or 120Ω applications. Each channel consists of a receiver with equalizer for reliable data and clock recovery, and a transmitter which accepts either a single or dual-rail digital inputs for signal transmission to the line using a low impedance line driver. The device also includes a crystal-less jitter attenuator which, depending on system requirement, can be selected in the receive or transmit path through the Host or Hardware Mode control.

The XRT82L38 can be configured as a 7 channel line interface with the eighth channel used for ITU-G.772 compliant protected monitoring purposes. This device uses a low power CMOS design and requires only a single 3.3V supply and all digital inputs are 5V tolerant.

FEATURES

- Fully integrated octal, short-haul PCM transceivers for T1 and E1 applications.
- On Chip Receive Equalizer and Transmit Pulse Shaper for DS1 Digital Cross Connect(DSX-1) and CEPT 75Ω and 120Ω line terminations
- On chip clock recovery circuit
- Transformer or capacitor coupled receiver inputs
- Crystal-less jitter attenuator can be selected in the transmit or receive path
- High receiver interference immunity
- Per-channel transmit power shutdown
- Tri-state transmit output capability
- Supports the same type transformer for both T1 and E1 line interface
- On chip per-channel driver failure monitoring circuit
- On chip HDB3/B8ZS/AMI encoder/decoder functions
- Transmit return loss meets or exceeds ETSI 300 166 standard
- Meets or exceeds specifications in ITU G.703, G.775, G.736 and G.823; Bellcore GR-499-CORE; ANSI T1.403 and ETSI 300-166
- JTAG Boundary Scan test port per IEEE1149.1
- G.772 Monitoring Capability
- Single +3.3V Supply Operation
- 3.3V or 5.0V Logic Level inputs
- 144-pin thermally enhanced TQFP Package

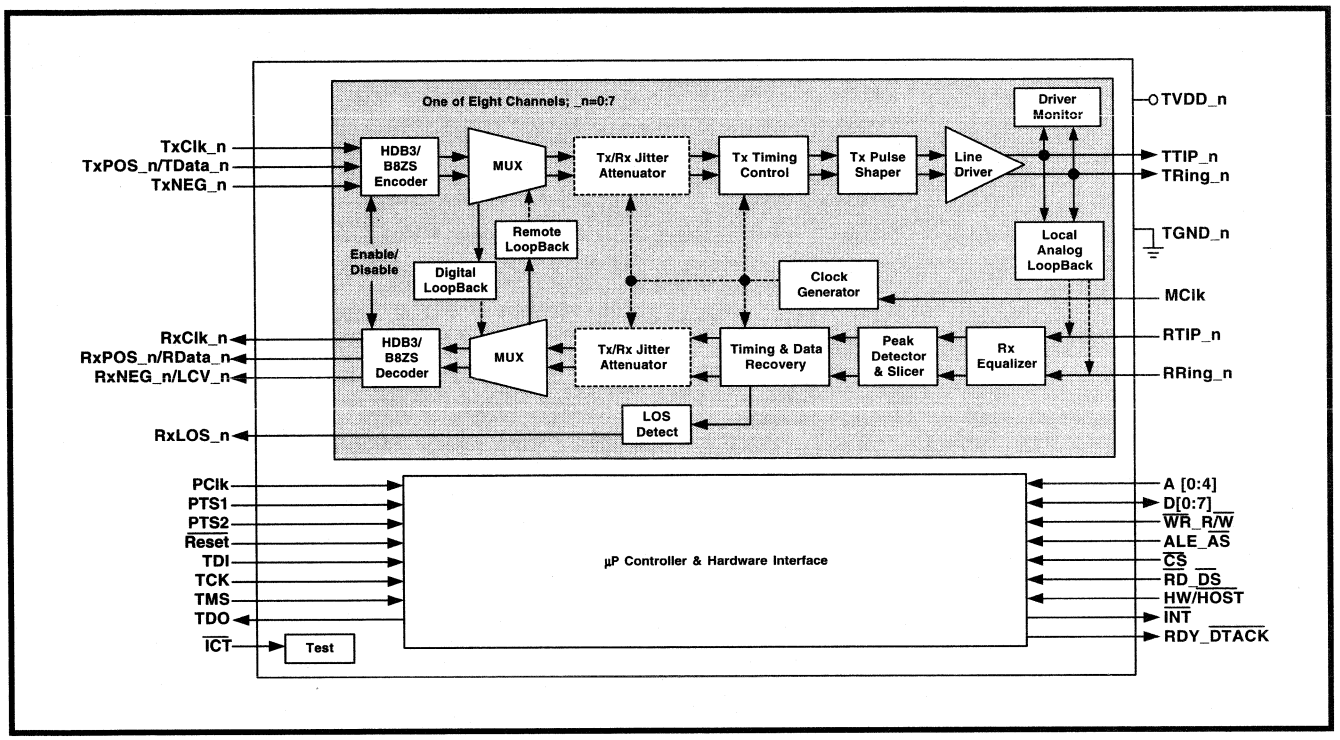
APPLICATIONS

- Digital cross connects(DSX-1)
- Channel Banks
- High speed data transmission line cards
- T1/E1 Multiplexer
- Public switching systems and PBX interfaces

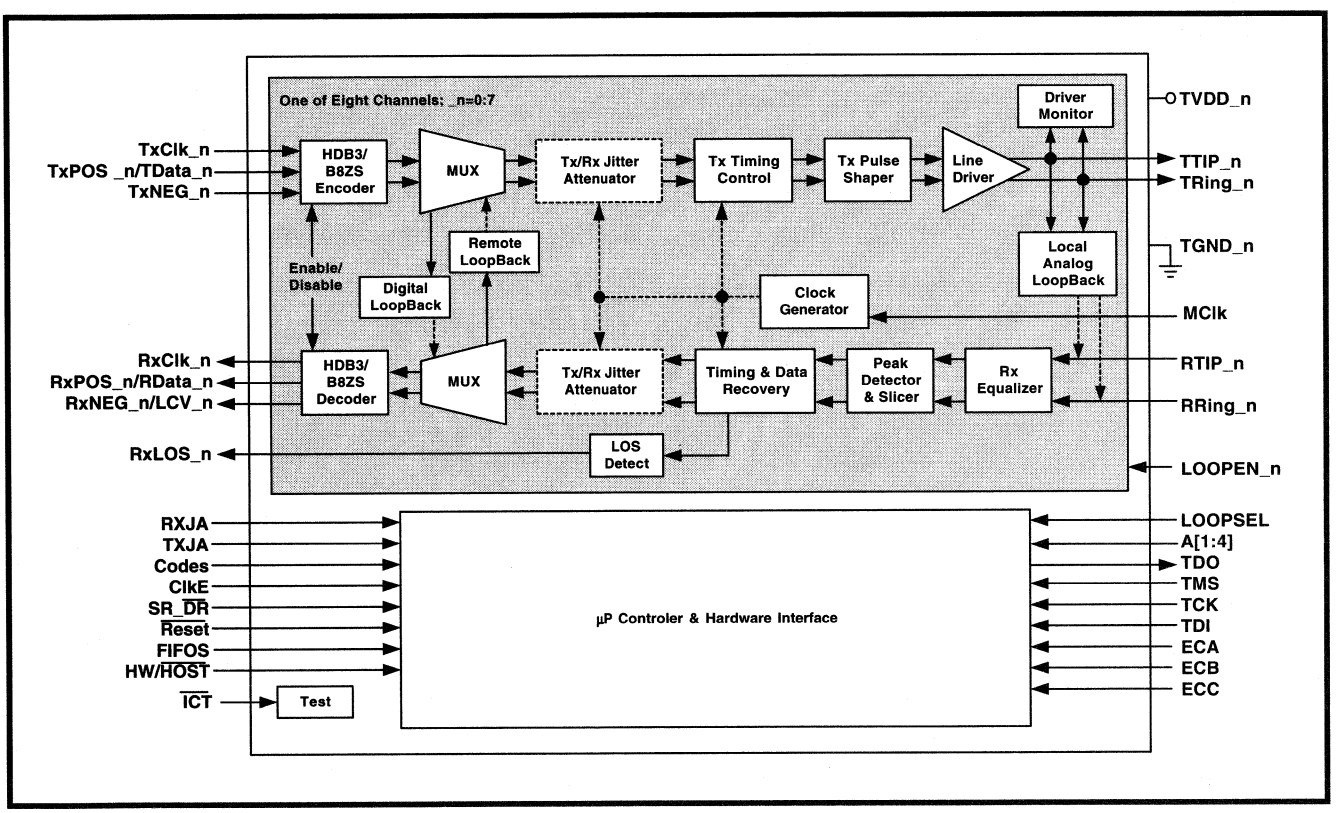
ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT82L38IV	144-LEAD TQFP (20 X 20 X 1.4MM)	-40°C TO +85°C

BLOCK DIAGRAM OF THE XRT82L38 IN HOST MODE



BLOCK DIAGRAM OF THE XRT82L38 IN HARDWARE MODE



GENERAL DESCRIPTION

The XRT83L30 is a fully integrated single-channel long-haul and short-haul line interface unit for T1(1.544Mbps) 100Ω, E1(2.048Mbps) 75Ω or 120Ω and J1 110Ω applications.

In long-haul applications the XRT83L30 accepts signals that have passed through cables from 0 feet to over 6000 feet in length and have been attenuated by 0 to 45dB at 772kHz in T1 mode or 0 to 43dB at 1024kHz in E1 mode. In T1 applications, the device generates five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB, -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generator that can be used for arbitrary output pulse shaping allowing performance improvement over a wide variety of conditions.

The XRT83L30 provides both Serial Host microprocessor interface and Hardware mode for programming and control. Both B8ZS and HDB3 encoding and decoding functions are included and can be disabled as required. On-chip crystal-less jitter attenuator (with a 32 or 64 bit FIFO) can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83L30 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. For the receiver this is accomplished by internal resistors or through the combination of one single fixed value external resistor and programmable internal resistors. In the absence of the power supply, the transmit output and receive input are tri-stated allowing for redundancy applications. The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

FEATURES

- Fully integrated single-channel long-haul or short-haul transceivers for E1, T1 or J1 applications.
- Adaptive Receive Equalizer for cable attenuation of up to 45dB for T1 and 43dB for E1.
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping.
- Programmable Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps.
- Tri-State transmit output and receive input capability for redundancy applications
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications.
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO Selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both Hardware and serial Microprocessor interface for programming
- 48-pin TQFP package
- -40°C to +85°C Temperature Range

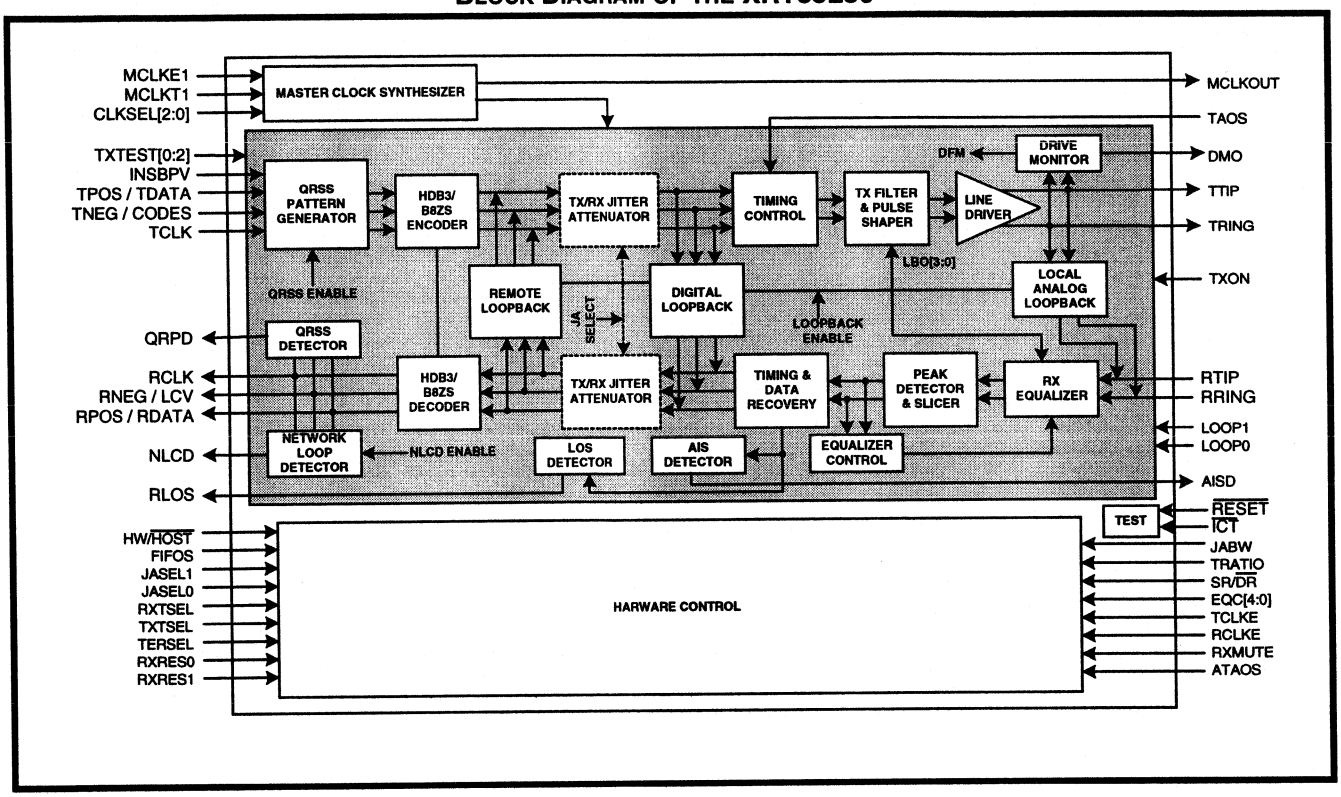
APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83L30IV	64-Lead TQFP (14 x 20 x 1.4 mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT83L30



GENERAL DESCRIPTION

The XRT83L34 is a fully integrated Quad (four channels) long-haul and short-haul line interface unit for T1(1.544Mbps) 100Ω, E1(2.048Mbps) 75Ω or 120Ω and J1 110Ω applications.

In long-haul applications the XRT83L34 accepts signals that have passed through cables from 0 feet to over 6000 feet in length and have been attenuated by 0 to 45dB at 772kHz in T1 mode or 0 to 43dB at 1024kHz in E1 mode. In T1 applications, the device generates five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB, -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions.

The XRT83L34 provides both parallel Host microprocessor interface and Hardware mode for programming and control. Both B8ZS and HDB3 encoding and decoding functions are included and can be disabled as required. On-chip crystal-less jitter attenuator (with a 32 or 64 bit FIFO) can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83L34 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. For each receiver this is accomplished through the combination of one single fixed value external resistor and programmable internal resistors. In the absence of the power supply, the transmit output and receive input are tri-stated allowing for redundancy applications. The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

FEATURES

- Fully integrated four channel long-haul or short-haul transceivers for E1, T1 or J1 applications.
- Adaptive Receive Equalizer for cable attenuation up to 45dB for T1 and 43dB for E1.
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping.
- Programmable Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps.
- Tri-State transmit output and receive input capability for redundancy applications
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications.
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO Selectable either in transmit or receive path
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both Hardware and parallel Microprocessor interface for programming
- Programmable Interrupt
- 128-pin TQFP package
- -40°C to +85°C Temperature Range

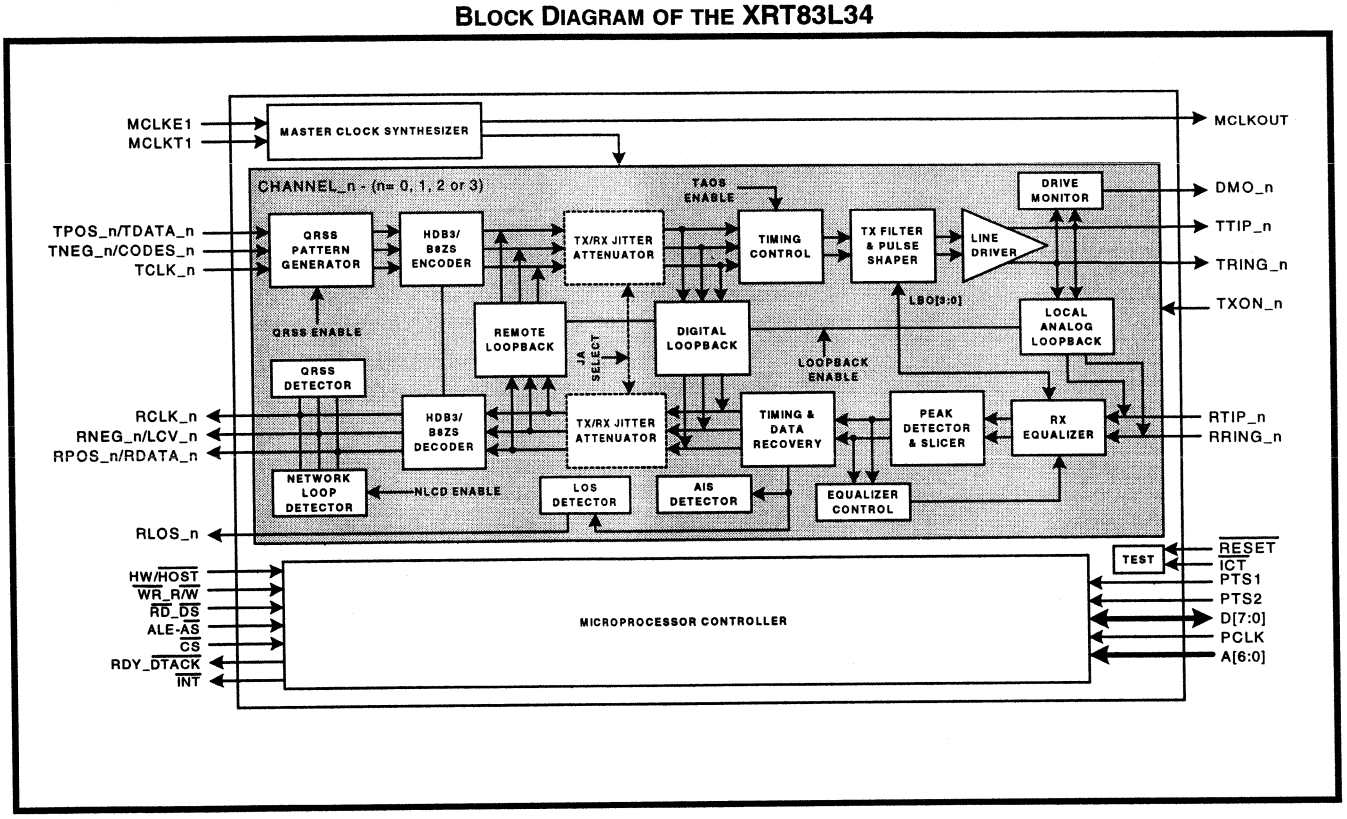
APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83L34IV	128-Lead TQFP (14 x 20 x 1.4 mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT83L34



GENERAL DESCRIPTION

The XRT83L38 is a fully integrated Octal (eight channels) long-haul and short-haul line interface unit for T1(1.544Mbps) 100Ω, E1(2.048Mbps) 75Ω or 120Ω and J1 110Ω applications.

In long-haul applications the XRT83L38 accepts signals that have passed through cables from 0 feet to over 6000 feet in length and have been attenuated by 0 to 45dB at 772kHz in T1 mode or 0 to 43dB at 1024kHz in E1 mode. In T1 applications, the XRT83L38 can generate five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB,-15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions.

The XRT83L38 provides both a parallel Host microprocessor interface as well as a Hardware mode for programming and control. Both the B8ZS and HDB3 encoding and decoding functions are included and can be disabled as demanded by the system. An on-chip crystal-less jitter attenuator with a 32 or 64 bit FIFO can be placed either in the receive or the transmit path with loop bandwidths of less than 3Hz. The XRT83L38 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. For each receiver this is accomplished through the combination of one single fixed value external resistor and programmable internal resistors. In the absence of the power supply, the transmit output and receive input are tri-stated allowing for redundancy applications The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master clocks from a variety of external clock sources.

FEATURES

- Fully integrated eight channel long-haul or short-haul transceivers for E1, T1 or J1 applications.
- Adaptive Receive Equalizer for up to 45dB cable attenuation.
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping.
- Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps.
- Selectable receiver sensitivity from 0 to 36dB or 0 to 45dB cable loss for T1 @772kHz and E1 @1024kHz.
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications.
- Tri-State transmit output and receive input capability for redundancy applications
- On-chip frequency multiplier generates T1 or E1 Master clocks from variety of external clock sources
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)
- Supports Analog, Remote, Digital and Dual Loop-Back Modes
- Supports both Hardware and Host (parallel Microprocessor) interface for programming
- 208-pin QFP package
- -40°C to +85°C Temperature Range

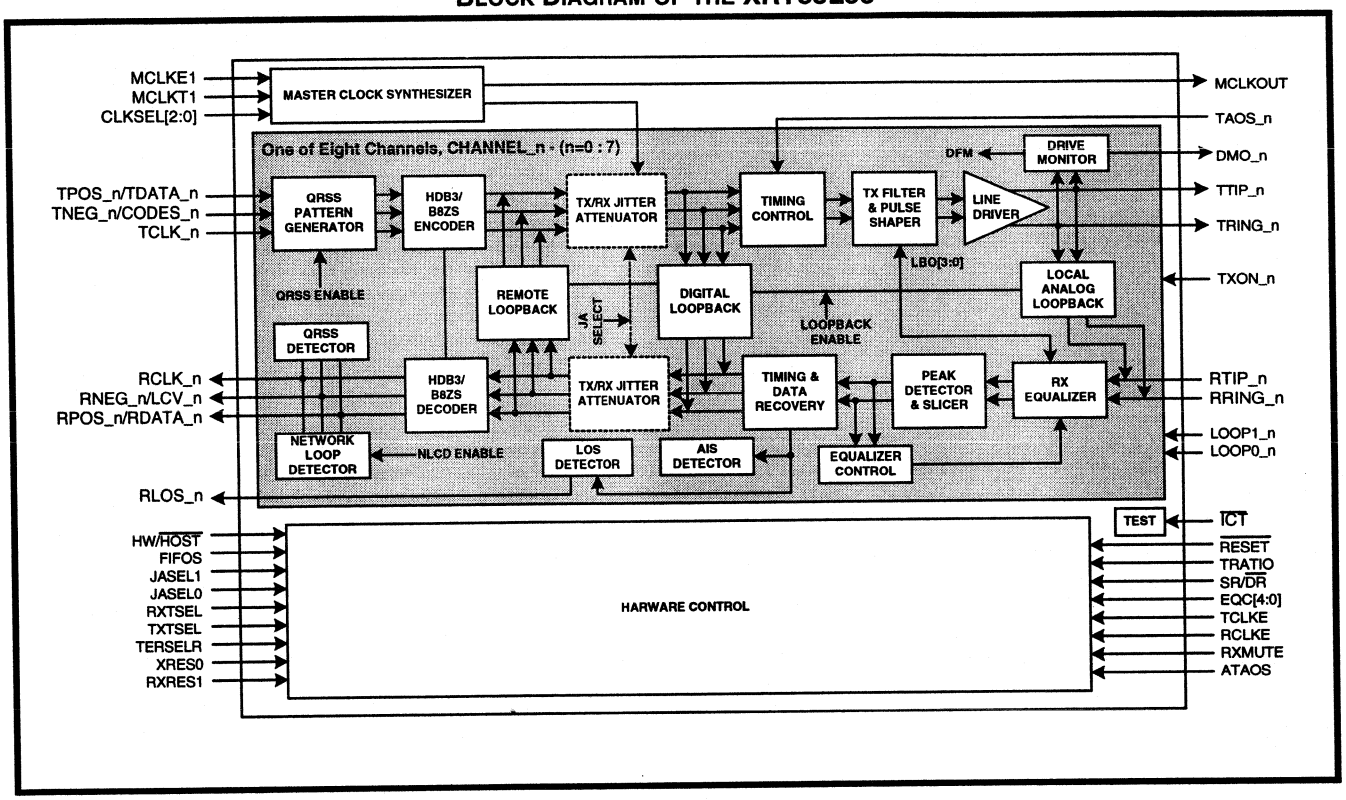
APPLICATIONS

- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83L38IV	208-Lead TQFP (28 x 28 x 1.4mm)	-40°C to +85°C

BLOCK DIAGRAM OF THE XRT83L38



GENERAL DESCRIPTION

The XRT84L14 quad T1 Framer contains four DS1/ ISDN-PRI fully independent DS1 framing transceivers for D4, ESF, Non-signaling (N), T1DM and SLC-96 ® formats. Each framer has its own framing synchronizer and transmit-receive slip buffers that can be independently enabled and disabled as required and configured and read through a common 8-bit µP parallel port.

Each Framer block contains its own Transmit and Receive DS1 Framing function and a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound DS1 frames Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound DS1 frames. The Transmit HDLC controller encapsulates contents of the Transmit HDLC buffers into LAPD Message frames. The Receive HDLC controller extracts payload content of Receive LAPD Message frames from the incoming T1 data stream and writes it into the Receive HDLC buffer. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, loopback codes and forced error insertion.

FEATURES

- Four independent, full duplex T1, Tx, and Rx Framer
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx
- Provides up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data from 1.544 to 8.192 MHz. Also supports 4-channel multiplexed 12.352/16.384 Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1
- Supports channel associated signaling (CAS)
- Supports Common-channel and ISDN Primary Rate Interface (ISDN PRI) signaling
- Integrated HDLC controller with two 96-byte Transmit HDLC buffers and two 96-byte Receive HDLC buffers
- Timeslot assignable HDLC
- Programmable Interrupt output pin
- Supports programmed I/O, Burst and DMA modes of Read-Write access
- Facilitates Inverse Multiplexing for ATM
- Extracts and inserts robbed bit signaling (RBS)
- 8-bit Intel/Motorola µP interface for configuration, control and status monitoring
- Dual or single rail line side digital PCM inputs
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Accepts external 8kHz Sync reference
- Fully meets all of the latest T1 specifications: ANSI T1.403-1995, ANSI T1.231-1993, AT&T TR62411 (12-90), AT&T TR54016 and TR62411, and ITU G-703, G.704, G706 and G.733.3.3V CMOS operation with 5V tolerant inputs
- Pin-compatible with the XRT84V24, 4-channel E1 framer

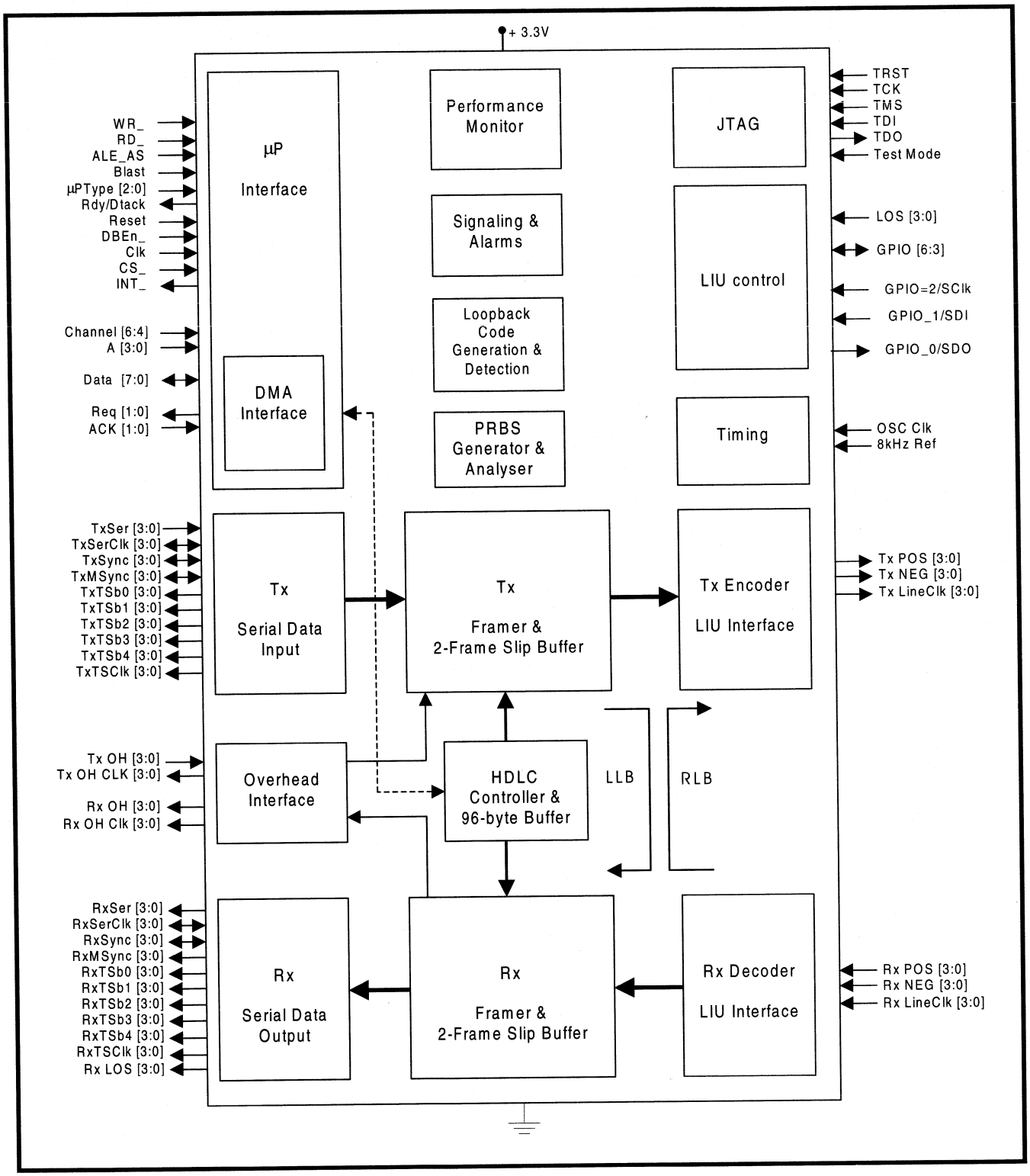
APPLICATIONS

- High-Density T1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1 and Fractional T1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated T1 interfaces

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT84L14IQ	208-Lead PQFP	-40°C to +85°C

XRT84L14 BLOCK DIAGRAM



EIGHT-CHANNEL T1 FRAMER

GENERAL DESCRIPTION

The XRT84L18 octal T1 Framer is a single chip device which integrates 8 T1 framers and transmitters for terminating DS1 Signals. Each framer has its own framing synchronizer and transmit-receive slip bufffers, and can be independently enabled or disabled as required and can be configured to frame to the common DS1 signal formats.

Each Framer block contains its own Transmit and Receive DS1 Framing function. The Transmit HDLC controller encapsulates contents of the Transmit HDLC buffers into LAPD Message frames. The Receive HDLC controller extracts payload content of Receive LAPD Message frames from the incoming T1 data stream and writes it into the Receive HDLC buffer. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound DS1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound DS1 frames.

The XRT84L18 fully meets all of the latest T1 specifications: ANSI T1.403-1995, ANSI T1.231-1993, AT&T TR62411 (12-90), AT&T TR54016 and TR62411, and ITU G-703, G.704, G706 and G.733. Extensive test and diagnostic functions include Loopbacks, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, and forced error insertion.

FEATURES

- Eight independent, full duplex T1, Tx, and Rx Framers
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data from 1.544 to 8.192 MHz. Also supports 4-channel multiplexed 12.352/16.384 Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1
- Supports channel associated signaling (CAS)
- Extracts and inserts robbed bit signaling (RBS)
- Supports Common-channel and ISDN Primary Rate Interface (ISDN PRI) signaling
- Integrated HDLC controller with two 96-byte Transmit HDLC buffers and two 96-byte Receive HDLC buffers
- Timeslot assignable HDLC
- 8-bit Intel/Motorola µP interface for configuration, control and status monitoring
- Programmable Interrupt output pin
- Supports programmed I/O, Burst and DMA modes of Read-Write access
- Dual or single rail line side digital PCM inputs
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Accepts external 8kHz Sync reference
- 3.3V CMOS operation with 5V tolerant inputs
- 4-channel T1 framer version (XRT84L14) is pin-compatible with the XRT84V24, 4-channel E1 framer

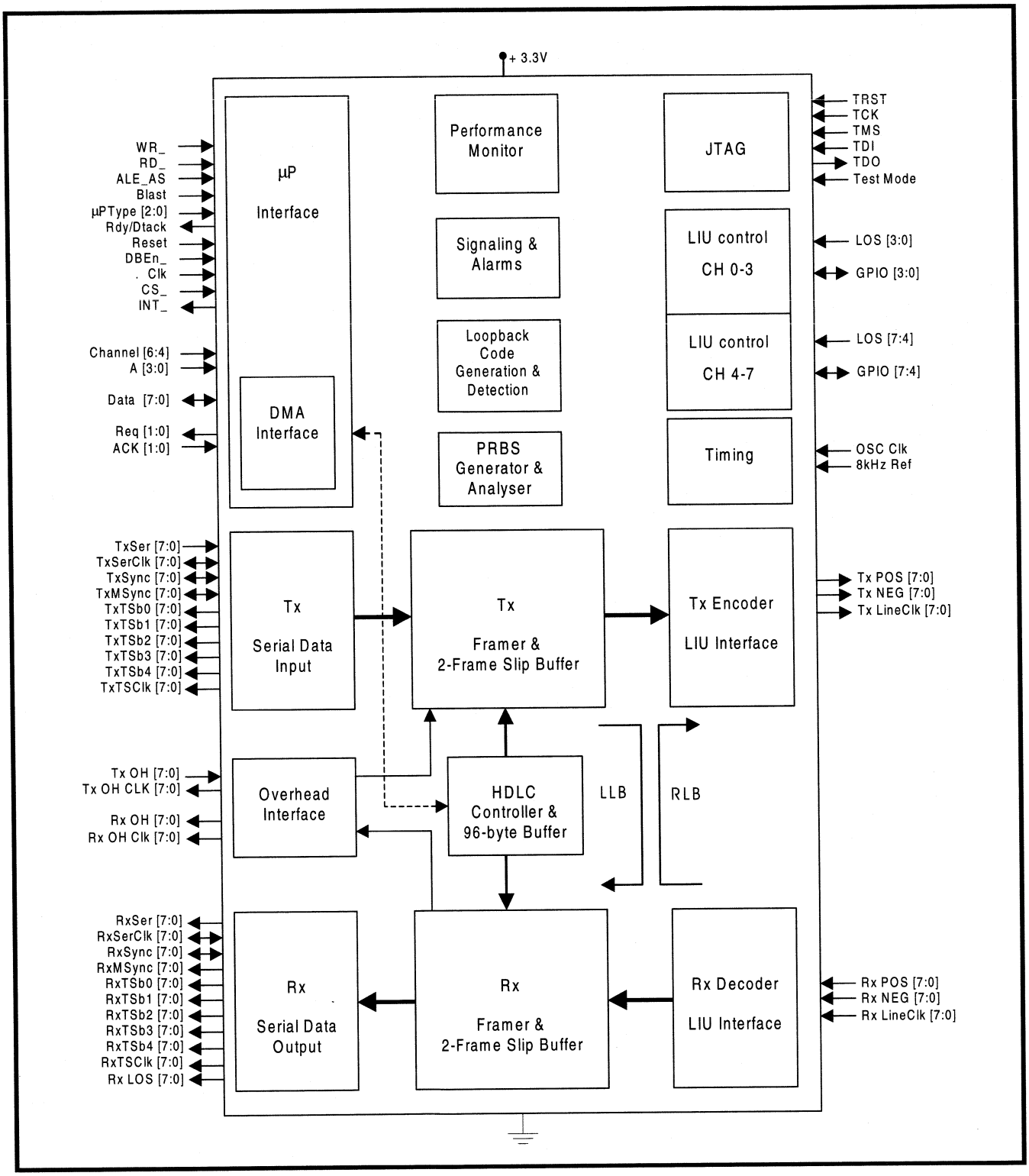
APPLICATIONS

- High-Density T1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1 and Fractional T1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated T1 interfaces

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT84L18IB	388-Ball PBGA (35 x 35mm)	-40°C to +85°C

XRT84L18 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT84V24 Quad E1 Framer IC contains four independent E1 Framer blocks. Each E1 Framer block contains its own Transmit and Receive E1 Framing function, Transmit HDLC Controller (which encapsulates contents of Transmit HDLC Buffers into LAPD Message frames) and Receiver HDLC Controller (which extracts payload content of "Receive LAPD Message" frames from the incoming E1 data stream and writes it into the Receive HDLC Buffer). Each framer also contains a Transmit and Overhead Input port, which permits "Data Link" Terminal equipment direct access to the outbound E1 frames and a Receive Overhead Output port, which permits "Data Link" Terminal equipment direct access to the "Data Link" bits within the inbound E1 frames.

FEATURES

- Four independent, ITU-T G.704 compliant Transceiver E1 Framers
- Supports Channel Associated Signaling
- Supports Common-Channel and Primary Rate ISDN Signaling
- Supports FAS, CRC-Multiframe and CAS Multiframe framing stuctures
- Contains two 96 byte Transmit HDLC Buffers and two 96 byte Receive HDLC buffers for each channel
- Contains Microprocessor Interface for popular types of Microprocessors and supports Programmed I/O, Burst and DMA modes of Read/Write access
- Each framer block can encode or decode the E1 Frame data into/from the Single-Rail or Dual-Rail (AMI or HDB3 encoded) formats
- Detects and forces RAI and AIS Alarms
- Detects LOF, COFA and LOS conditions
- Each Framer Contains a 512 bit Elastic Store Buffer
- Uses a Single +3.3V Power Supply
- Available in a 208-pin PQFP package

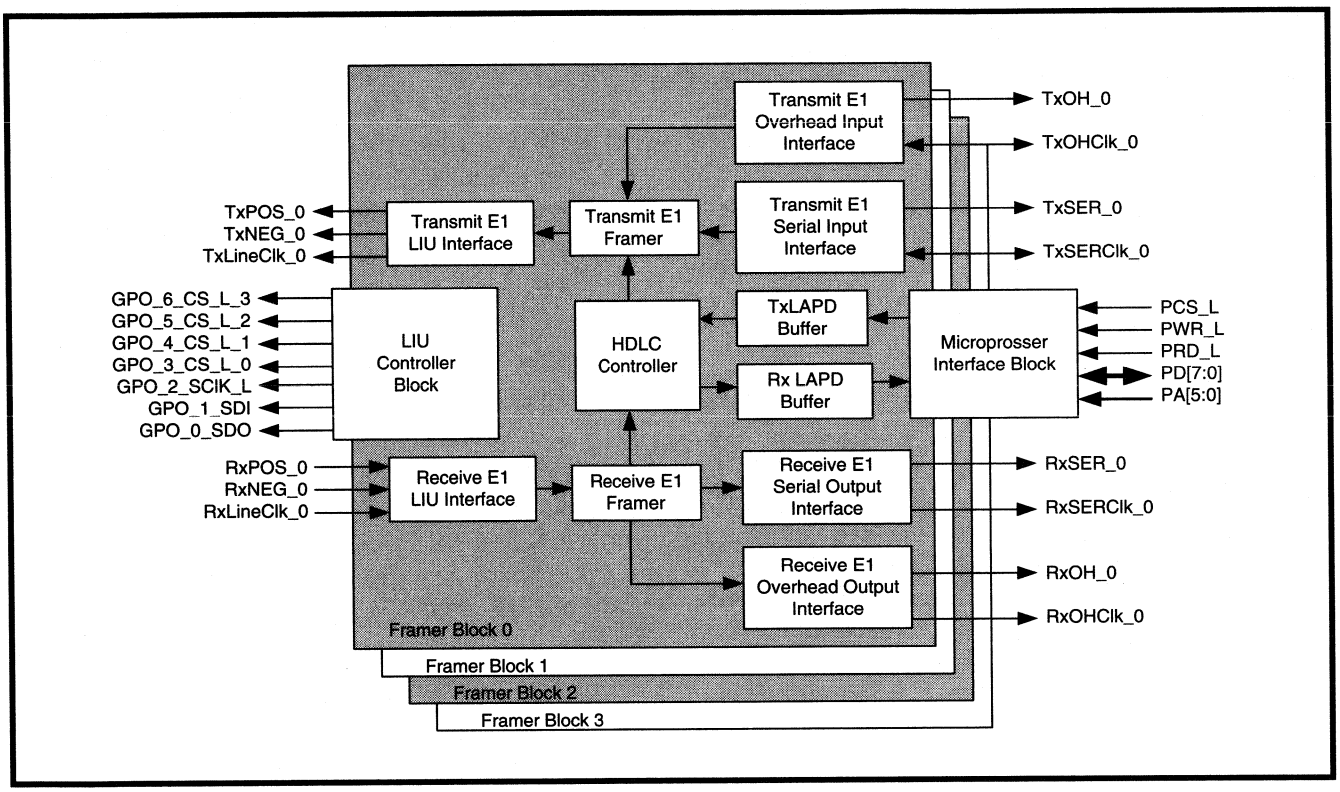
APPLICATIONS

- SDH terminal or add/drop multiplexers supporting E1 framing
- E1 multiplexers
- Channel Service Units (CSUs)
- LAN routers with integrated E1 interfaces
- E1 Frame Relay Interface
- ISDN Primary Rate Interfaces
- Test Equipment

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT84V24IV	208-Lead PQFP	-40° C to +85° C

XRT84V24 BLOCK DIAGRAM



EIGHT-CHANNEL T1/E1/J1 FRAMER

GENERAL DESCRIPTION

The XRT84L38 is an eight-channel 1.544 Mbit/s or 2.048 Mbit/s T/E1/J1 framing controller. The XRT84L38 contains an integrated T1/E1/J1 framer which provides T1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip bufffers, and can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. The Transmit HDLC controller encapsulates contents of the Transmit HDLC buffers into LAPD Message frames. The Receive HDLC controller extracts payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and writes it into the Receive HDLC buffer. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT84L38 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

FEATURES

- Eight independent, full duplex DS1 Tx and Rx Framers
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data from 1.544 to 8.192 MHz. Also supports 4-channel multiplexed 12.352/16.384 Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- Integrated HDLC controller with two 96-byte Transmit HDLC buffers and two 96-byte Receive HDLC buffers
- Timeslot assignable HDLC
- 8-bit Intel/Motorola µP interface for configuration, control and status monitoring
- Programmable Interrupt output pin
- Supports programmed I/O, Burst and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/E1/J1 Frame serial data into and from the Single-rail or Dual-rail (B8ZS) format
- Dual or single rail line side digital PCM inputs
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 3.3V CMOS operation with 5V tolerant inputs
- 388-ball BGA package with –40° C to +85° C operation
- Direct Interface to Exar's LIUs: XRT82L38 (Octal) and XRT82L34 (Quad)

APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)

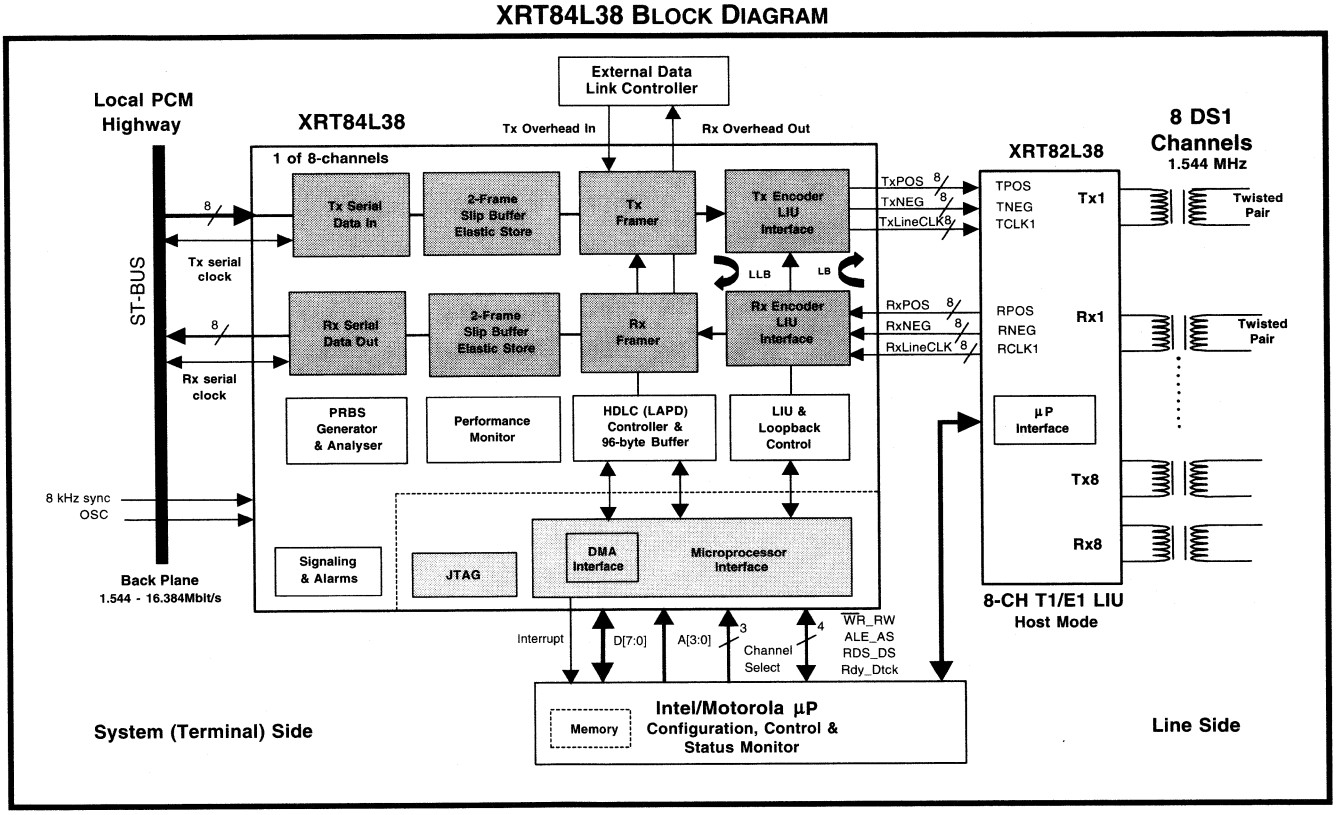
APPLICATIONS (CONT'D)

- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT84L38	388-Ball PBGA	-40^{0}C to +85^{0}C

XRT84L38 BLOCK DIAGRAM



SONET/SDH STS-12/STM-4 TO E3/DS3/STS-1 MAPPER/DEMAPPER

REV. P1.0.0

GENERAL DESCRIPTION

The XRT94L43 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-12 or STM-4 data stream. The XRT94L43 interfaces to either STS-12 or STM-4 signals using a byte wide parallel inter-face in Telecom Bus format or via serial line interface that operates at 622.08 MHz.

The XRT94L43 processes the section,line and path overhead in the SONET/SDH data stream. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface

The XRT94L43 uses th
chronizer circuit with ar
rithm for clock smoothing
ter due to mapping and
De-Synchronizer circuits
clock reference for its op

The SONET/SDH transm
tion of TOH and POH by
and Software. Individual
ted SONET/SDH signal
XRT94L43 memory map
A1,A2 framing pattern,
byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing. The XRT94L43 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L43 provides 12 mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance. A general purpose microprocessor interface is included for control, configuration and monitoring.

The XRT94L43 block diagram is incorrect, please go to the bound-in CD, or to Exar's website at (http://www.exar.com/products/XRT94L43.html)

FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 12 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers.
- Generates and terminates SONET/SDH section, line and path layers.
- Integrated SERDES with Clock Recovery Circuit.
- Provides SONET frame scrambling and descrambling.
- Integrated Clock Synthesizer that generates 622.08 MHz and 77.76 MHz clock from an external 12.96/19.44/77.76 MHz reference clock.
- Provides STS-1 (EC1) mapping/de-mapping for up

3/STS-1 De-Synchronizer circped clock to meet 0.05UIpp jit-

ction DCC

Monitoring for E3 and DS3.

STS-1E and DS3 or E3 and

M-1 to STS-12/STM-4 Map-

for both Transmit and Receive

- Loopback support for both SONET/SDH as well as E3/DS3/STS-1.
- Boundary scan capability with JTAG IEEE 1149.1
- 8-bit microprocessor interface
- Power Supply 2.5 V for Core and 3.3 V for I/O
- -40°C to +85°C Operating Temperature Range
- Available in a 516 Ball PBGA package

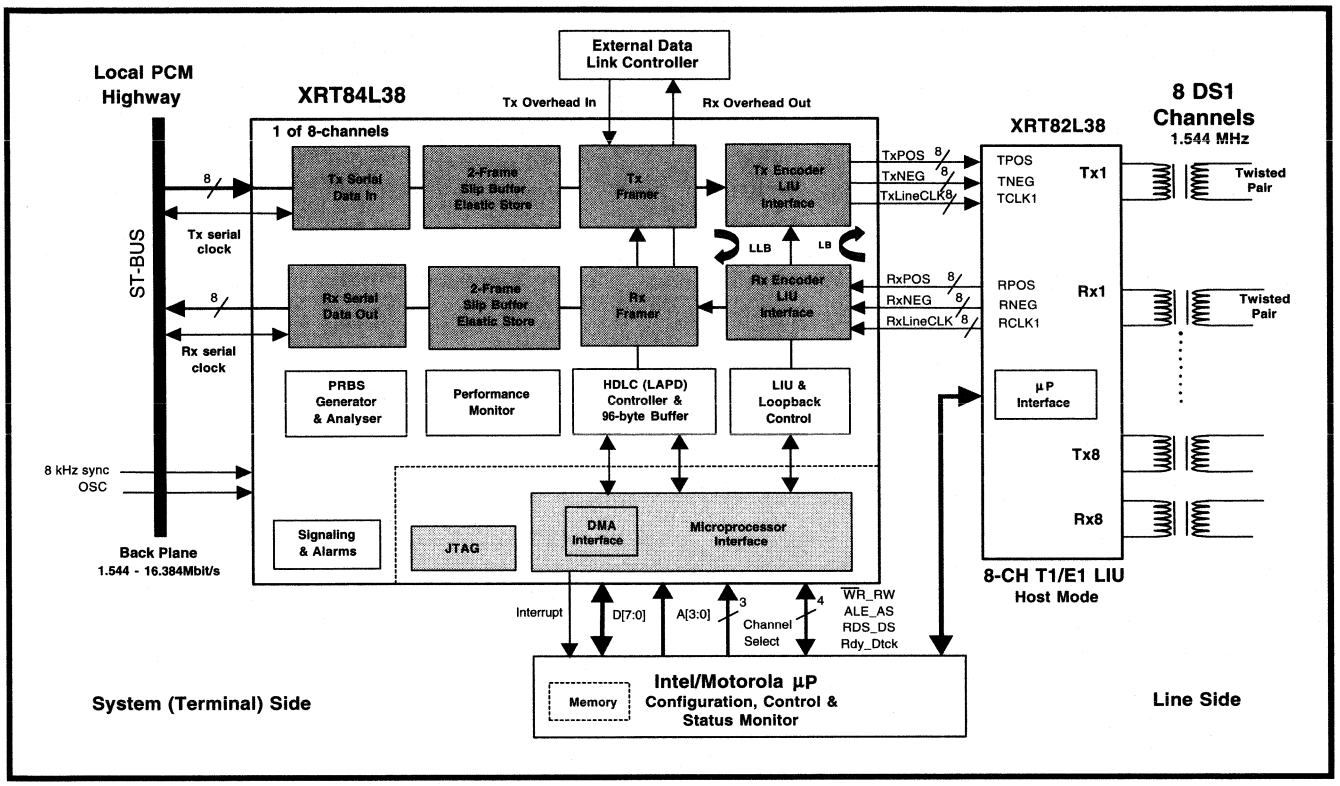
APPLICATIONS

- • Network switches
- • Add/Drop Multiplexer
- • W-DCS Digital Cross Connect Systems

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT94L43IB	516-Ball PBGA (35 x 35 mm)	-40^{0}C to +85^{0}C

XRT94L43 BLOCK DIAGRAM



GENERAL DESCRIPTION

The XRT95L51 is an ATM/PPP physical layer processor with integrated SONET OC-48/STM-16 framing controller. ATM direct mapping and cell delineation are supported, as are PPP mapping and frame processing. The XRT95L51 contains an integral SONET framer which provides framing and error accumulation in accordance with ANSI/ITU-T specifications. The configuration of this device is done through internal registers accessible via 8-bit parallel, memory mapped, microprocessor interface.

The XRT95L51 provides full section, line and path overhead processing and supports scrambling/descrambling, alarm signal insertion/detection and bit interleaved parity processing.

The SONET/SDH transmit and receive blocks are used to transmit/receive an OC-48c/STM-16c signal or compose and decompose four OC-12/12c signals.The blocks operate at a peak internal clock speed of 77 MHz and support 32-bit internal data paths. The transmit and receive blocks are compliant with both SONET and SDH standards.

FEATURES

- Single chip for ATM UNI and Packet over SONET.
- Generates and terminates SONET section, line and path layers.
- Provides SONET frame scrambling and descrambling.
- Provides 32-bit data UTOPIA level II and III multi-PHY interface and POS-PHY interface.
- 8-bit microprocessor interface
- Includes ATM cell or PPP packet mapping
- Single +3.3V power supply with +5V input tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 388-ball PBGA package

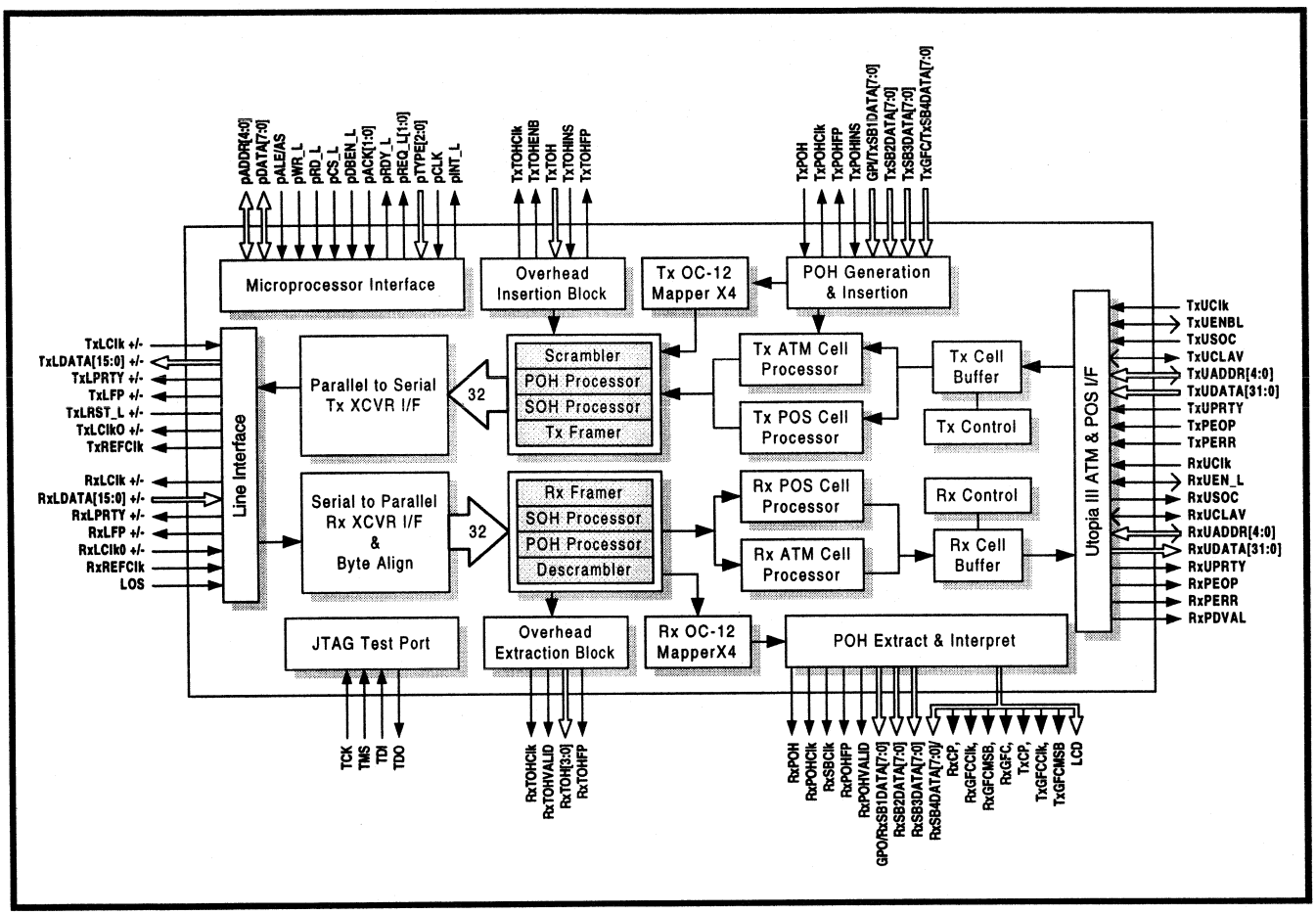
APPLICATIONS

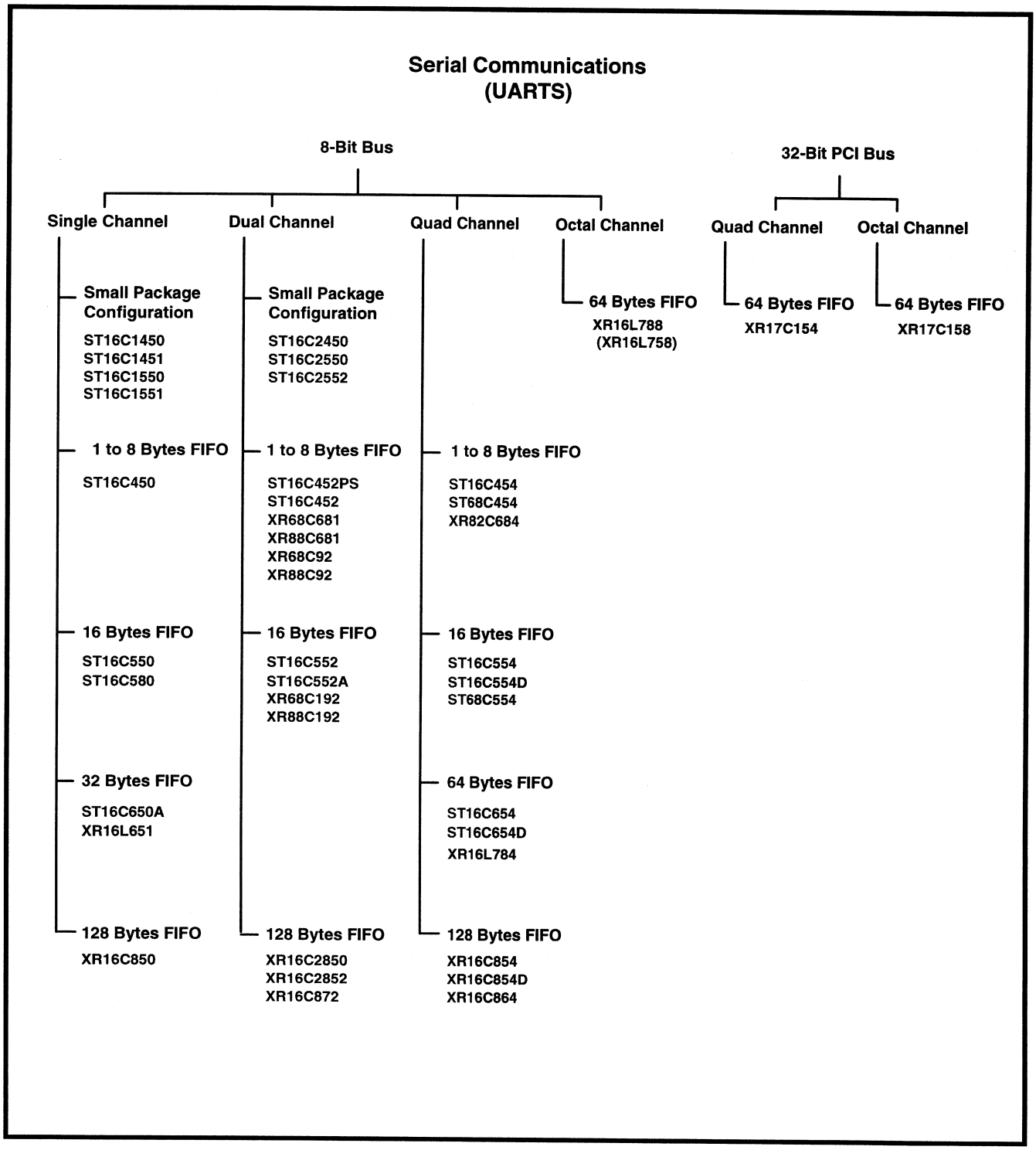
- Digital Cross Connect Systems
- ATM Switches
- Routers
- SONET/SDH Add Drop Multiplexers
- Multiplexers

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT95L51IB	388-Ball PBGA (35 x 35mm, 26 x 26 Ball Matrix)	-40°C to +85°C

XRT95L51 BLOCK DIAGRAM




Serial Communications
(UARTS)
8-Bit Bus
32-Bit PCI Bus
Single Channel
Dual Channel
Quad Channel
Octal Channel
Quad Channel
Octal Channel
Small Package Configuration
ST16C1450
ST16C1451
ST16C1550
ST16C1551
Small Package Configuration
ST16C2450
ST16C2550
ST16C2552
64 Bytes FIFO
XR16L788
(XR16L758)
64 Bytes FIFO
XR17C154
64 Bytes FIFO
XR17C158
1 to 8 Bytes FIFO
ST16C450
1 to 8 Bytes FIFO
ST16C452PS
ST16C452
XR68C681
XR88C681
XR68C92
XR88C92
1 to 8 Bytes FIFO
ST16C454
ST68C454
XR82C684
16 Bytes FIFO
ST16C550
ST16C580
16 Bytes FIFO
ST16C552
ST16C552A
XR68C192
XR88C192
16 Bytes FIFO
ST16C554
ST16C554D
ST68C554
32 Bytes FIFO
ST16C650A
XR16L651
64 Bytes FIFO
ST16C654
ST16C654D
XR16L784
128 Bytes FIFO
XR16C850
128 Bytes FIFO
XR16C2850
XR16C2852
XR16C872
128 Bytes FIFO
XR16C854
XR16C854D
XR16C864

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

DESCRIPTION

The ST16C1450, ST16C1451 series is a universal asynchronous receiver and transmitter (UART). The ST16C1450/1451 is foot print compatible to the SSI 73M1550 UART with one byte FIFO and higher operating speed and lower access time. The ST16C1450/1451 provides enhanced UART functions with a modem control interface and independent programmable baud rate generators with clock rates to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loop-back capability allows onboard diagnostics. The ST16C1450/1451 is available in a 28-pin PLCC/PDIP and 48-pin TQFP packages. The baud rate generator can be configured for either crystal or external clock input with the exception of the 28 pin 1451 package. An external clock must be provided for the 28 pin 1451 package. Each package type, with the exception of the 28 pin 1450, provides a buffered reset output that can be controlled through user software. The ST16C1450/1451 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

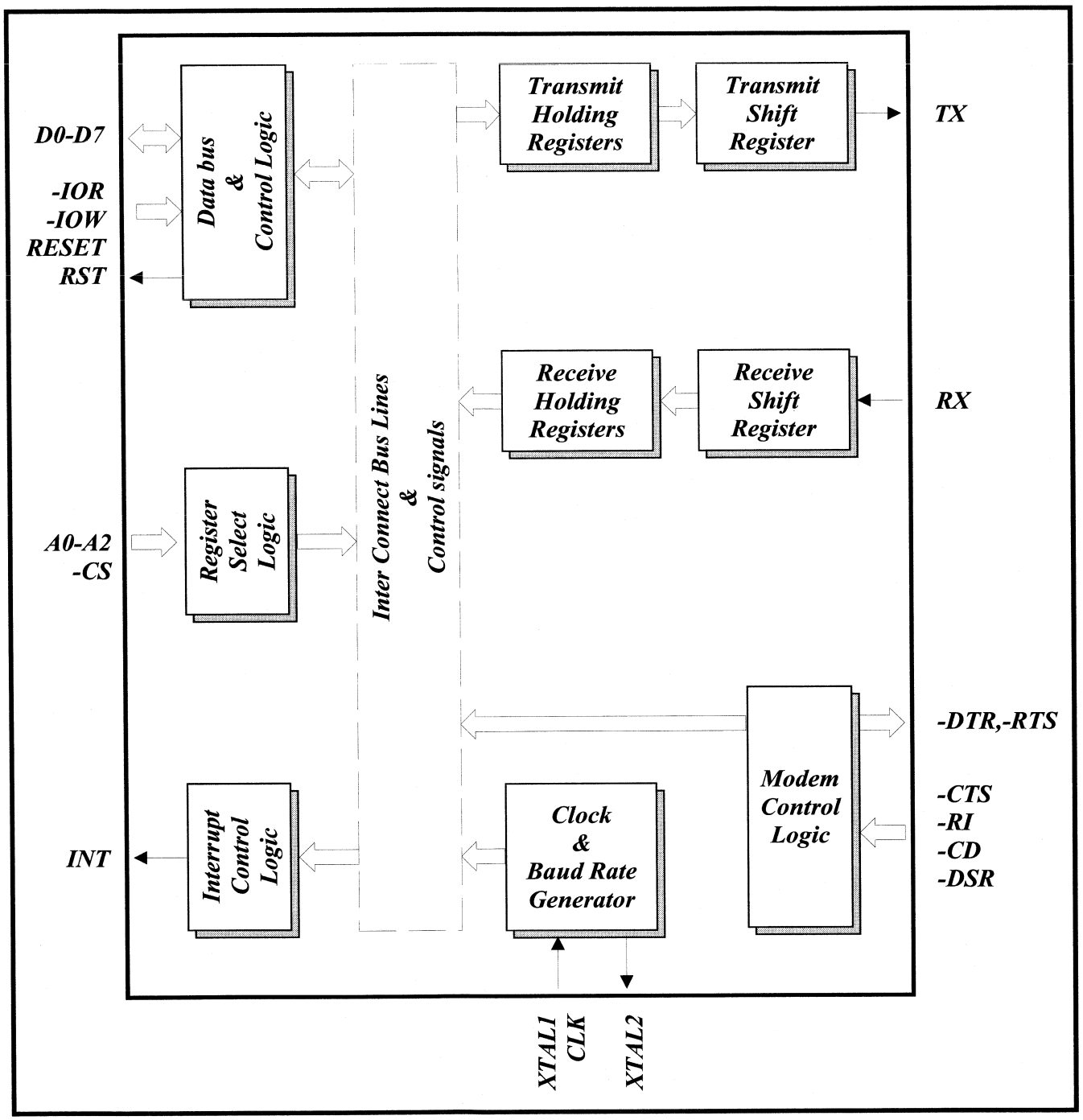
FEATURES

- Pin compatible to SSI 73M1550
- 1.5 Mbps transmit/receive operation (24MHz Max.) with programmable clock control
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8) with Even, odd, or no parity
- Four levels of prioritized interrupts, minimize external software interaction
- Software controlled tri-state interrupt outputs
- Provides enhanced 16C450 features for power down and software controllable reset output
- Crystal or external clock input (except 28 pin ST16C1451)
- 460.8 Kbps transmit/receive operation with 7.3728 MHz crystal or external clock source

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C1450CP28	28-Lead PDIP	0°C to + 70°C
ST16C1450CJ28	28-Lead PLCC	0°C to + 70°C
ST16C1450CQ48	48-Lead TQFP	0°C to + 70°C
ST16C1451CP28	28-Lead PDIP	0°C to + 70°C
ST16C1451CJ28	28-Lead PLCC	0°C to + 70°C
ST16C1451CQ48	48-Lead TQFP	0°C to + 70°C
ST16C1450IP28	28-Lead PDIP	-40°C to + 85°C
ST16C1450IJ28	28-Lead PLCC	-40°C to + 85°C
ST16C1450IQ48	48-Lead TQFP	-40°C to + 85°C
ST16C1451IP28	28-Lead PDIP	-40°C to + 85°C
ST16C1451IJ28	28-Lead PLCC	-40°C to + 85°C
ST16C1451IQ48	48-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



DESCRIPTION

The ST16C1550, ST16C1551 series (here in denoted as the 155X) is a universal asynchronous receiver and transmitter (UART). The 155X is an improved version of the SSI 73M1550 UART with higher operating speed and lower access time. The 155X provides enhanced UART functions with 16 byte FIFOs, a modem control interface and independent programmable baud rate generators with clock rates to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loopback capability allows onboard diagnostics. The 155X is available in a 28-pin PLCC/PDIP and 48-pin TQFP packages. The baud rate generator can be configured for either crystal or external clock input with the exception of the 28 pin 1551 package. An external clock must be provided for the 28 pin 1551 package. Each package type, with the exception of the 28 pin 1550, provides a buffered reset output that can be controlled through user software. DMA monitor signals, TXRDY/RXRDY, are not available at the 155X I/O pins but these signals are accessible through ISR register bits 4-5. Except as listed above, each package version has the same features. The 155X is functionally compatible with the 16C550. The 155X is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

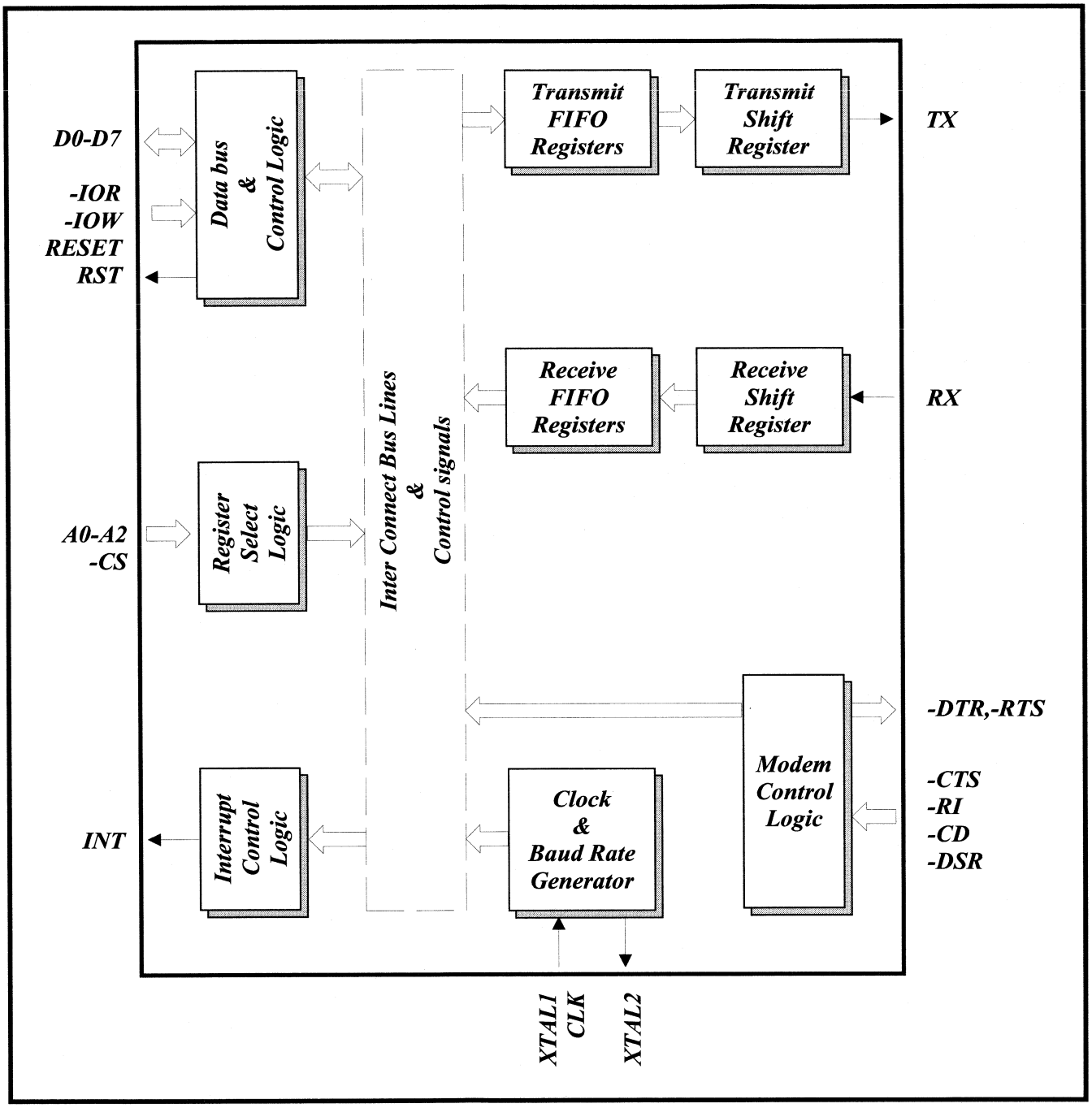
FEATURES

- ST16C1550/ST16C1551 are pin and functionally compatible to SSI 73M1550/2550
- 1.5 Mbps transmit/receive operation (24MHz Max.) with programmable clock control
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Four independently selectable Transmit and Receive FIFO interrupt trigger levels
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity
- Crystal or external clock input (except 28 pin ST16C1551)
- Provides enhanced 16C550 features for power down and software controllable reset output
- 460.8 Kbps transmit/receive operation with 7.3728MHz crystal or external clock source

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C1550CP28	28-Lead PDIP	0°C to + 70°C
ST16C1550CJ28	28-Lead PLCC	0°C to + 70°C
ST16C1550CQ48	48-Lead TQFP	0°C to + 70°C
ST16C1551CP28	28-Lead PDIP	0°C to + 70°C
ST16C1551CJ28	28-Lead PLCC	0°C to + 70°C
ST16C1551CQ48	48-Lead TQFP	0°C to + 70°C
ST16C1550IP28	28-Lead PDIP	-40°C to + 85°C
ST16C1550IJ28	28-Lead PLCC	-40°C to + 85°C
ST16C1550IQ48	48-Lead TQFP	-40°C to + 85°C
ST16C1551IP28	28-Lead PDIP	-40°C to + 85°C
ST16C1551IJ28	28-Lead PLCC	-40°C to + 85°C
ST16C155IQ48	48-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



DUAL ASYNCHRONOUS RECEIVER AND TRANSMITTER (UART)

DESCRIPTION

The ST16C2450 (2450) is a dual universal asynchronous receiver and transmitter (UART). The ST16C2450 is an improved version of the NS16450 UART with higher operating speed and lower access time. The 2450 provides enhanced UART functions with a modem control interface, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loop-back capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50 Bps to 1.5 Mbps. The baud rate generator can be configured for either crystal or external clock input. The 2450 is available in a 40-pin PDIP, 44-pin PLCC and 48-pin TQFP packages. The 2450 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

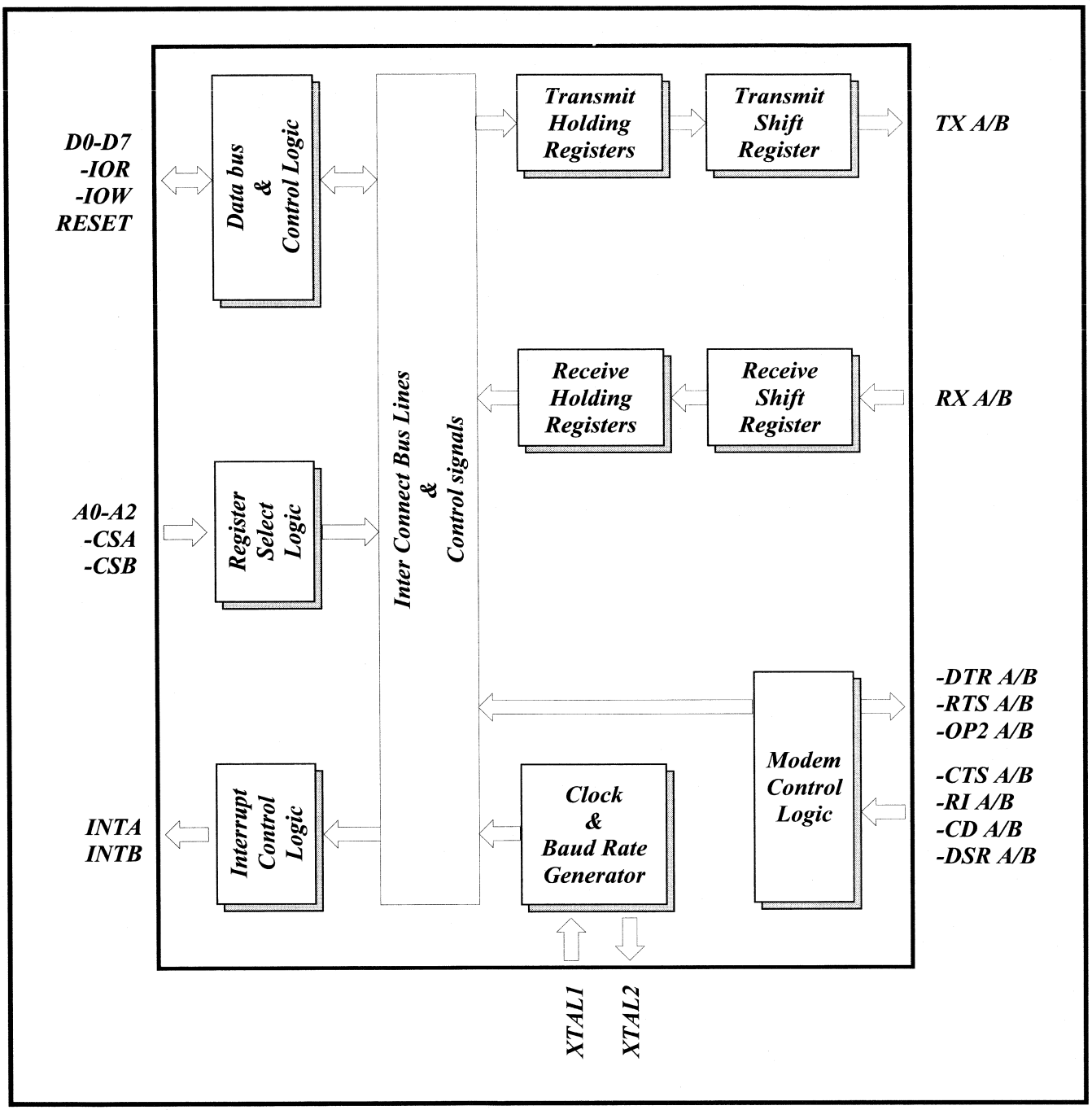
FEATURES

- Pin and functionally compatible to the ST16C2550
- Software compatible with INS8250/16C450
- 1.5 Mbps transmit/receive operation (24MHz Max.)
- Independent transmit and receive UART control
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity
- Status report register
- Crystal or external clock input
- 460.8 Kbps transmit/receive operation with 7.3728 MHz crystal or external clock source
- TTL compatible inputs, outputs

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C2450CP40	40-Lead PDIP	0°C to + 70°C
ST16C2450CJ44	44-Lead PLCC	0°C to + 70°C
ST16C2450CQ48	48-Lead TQFP	0°C to + 70°C
ST16C2450IP40	40-Lead PDIP	-40°C to + 85°C
ST16C2450IJ44	44-Lead PLCC	-40°C to + 85°C
ST16C2450IQ48	48-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



DUAL UART WITH 16-BYTE TRANSMIT AND RECEIVE FIFOs

DESCRIPTION

The ST16C2550 (2550) is a dual universal asynchronous receiver and transmitter (UART). The ST16C2550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The 2550 provides enhanced UART functions with 16 byte FIFOs, a modem control interface, and data rates up to 4Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loop-back capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50bps to 4Mbps with external clock. The baud rate generator can be configured for either crystal or external clock input. The 2550 is available in a 40-pin PDIP, 44-pin PLCC and 48-pin TQFP packages. The 40 pin package does not offer TXRDY and RXRDY pins (DMA Signal monitoring). Otherwise the three package versions are the same. The 2550 is functionally compatible with the 16C2450. The 2550 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

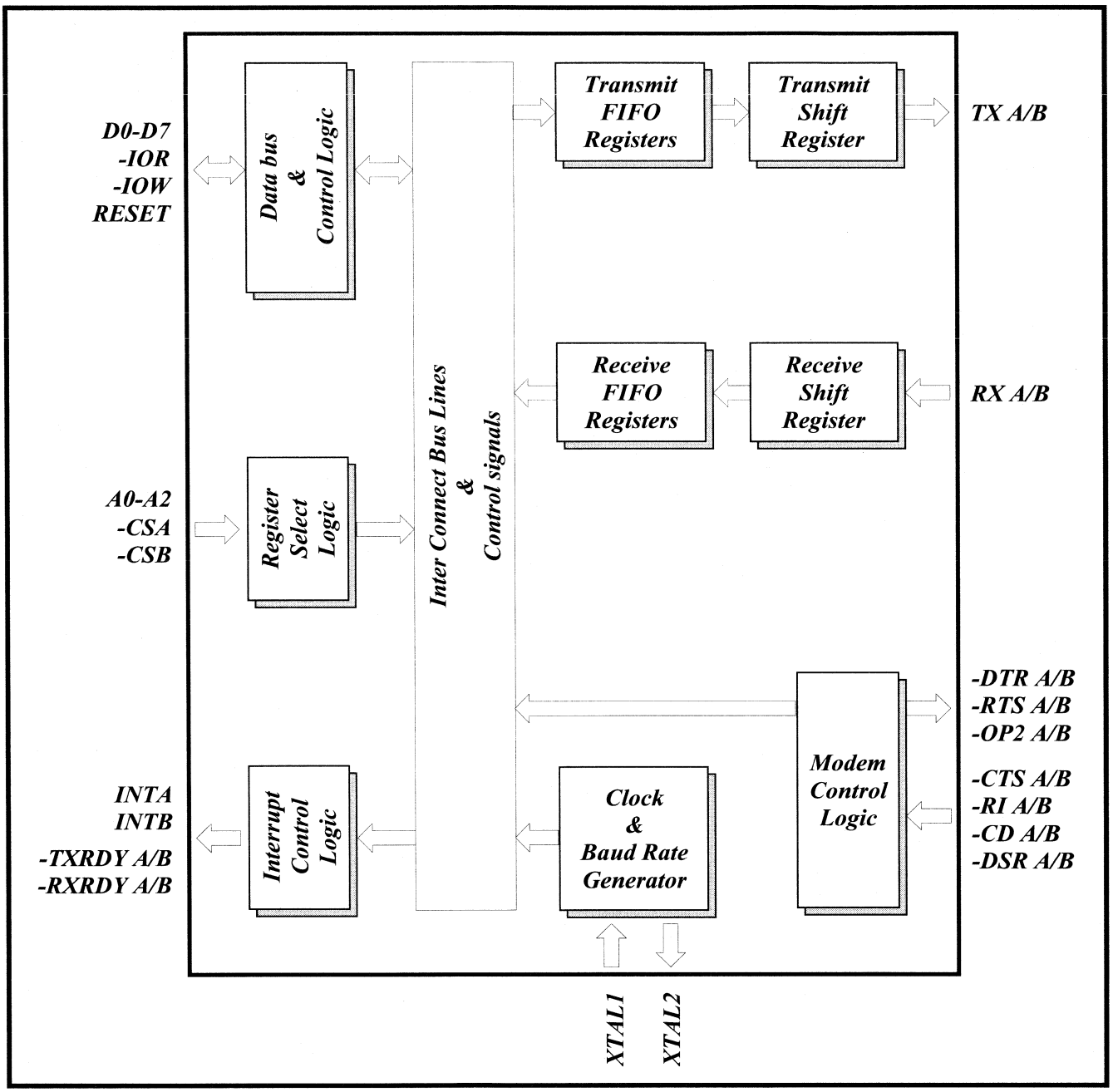
FEATURES

- Dual UART device
- Pin and functionally compatible to ST16C2450, software compatible with INS8250, NS16C550
- Up to 4Mbps with external clock of 64MHz
- Up to 1.5Mbps data rate with a 24MHz crystal frequency
- 16-byte transmit FIFO to reduce the bandwidth requirement of the external CPU
- 16-byte receive FIFO with error flags to reduce the bandwidth requirement of the external CPU
- Independent transmit and receive UART control
- Four selectable Receive FIFO interrupt trigger levels
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD, and Software controllable line break)
- Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity
- Status report register
- Crystal or external clock input
- TTL compatible inputs, outputs
- 3.3V or 5V supply operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C2550CP40	40-Lead PDIP	0°C to + 70°C
ST16C2550CJ44	44-Lead PLCC	0°C to + 70°C
ST16C2550CQ48	48-Lead TQFP	0°C to + 70°C
ST16C2550IP40	40-Lead PDIP	-40°C to + 85°C
ST16C2550IJ44	44-Lead PLCC	-40°C to + 85°C
ST16C2550IQ48	48-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



DUAL UART WITH 16-BYTE TRANSMIT AND RECEIVE FIFOs

REV. 3.50

DESCRIPTION

The ST16C2552 (2552) is a dual universal asynchronous receiver and transmitter (UART). The ST16C2552 is an improved version of the NS16C552/PC16552 UART. The 2552 provides enhanced UART functions with 16 byte FIFO's, a modem control interface, and data rates up to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loop-back capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50 Bps to 1.5 Mbps. The baud rate generator can be configured for either crystal or external clock input. The 2552 is available in 44 pin PLCC packages. The 2552 provides block mode data transfers (DMA) through FIFO controls. DMA transfer monitoring is provided through the signals -TXRDY and -RXRDY. An Alternate Function Register provides the user with the ability to the write the control registers for both UARTS concurrently. The 2552 is functionally compatible with the NS16C552. The 2552 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

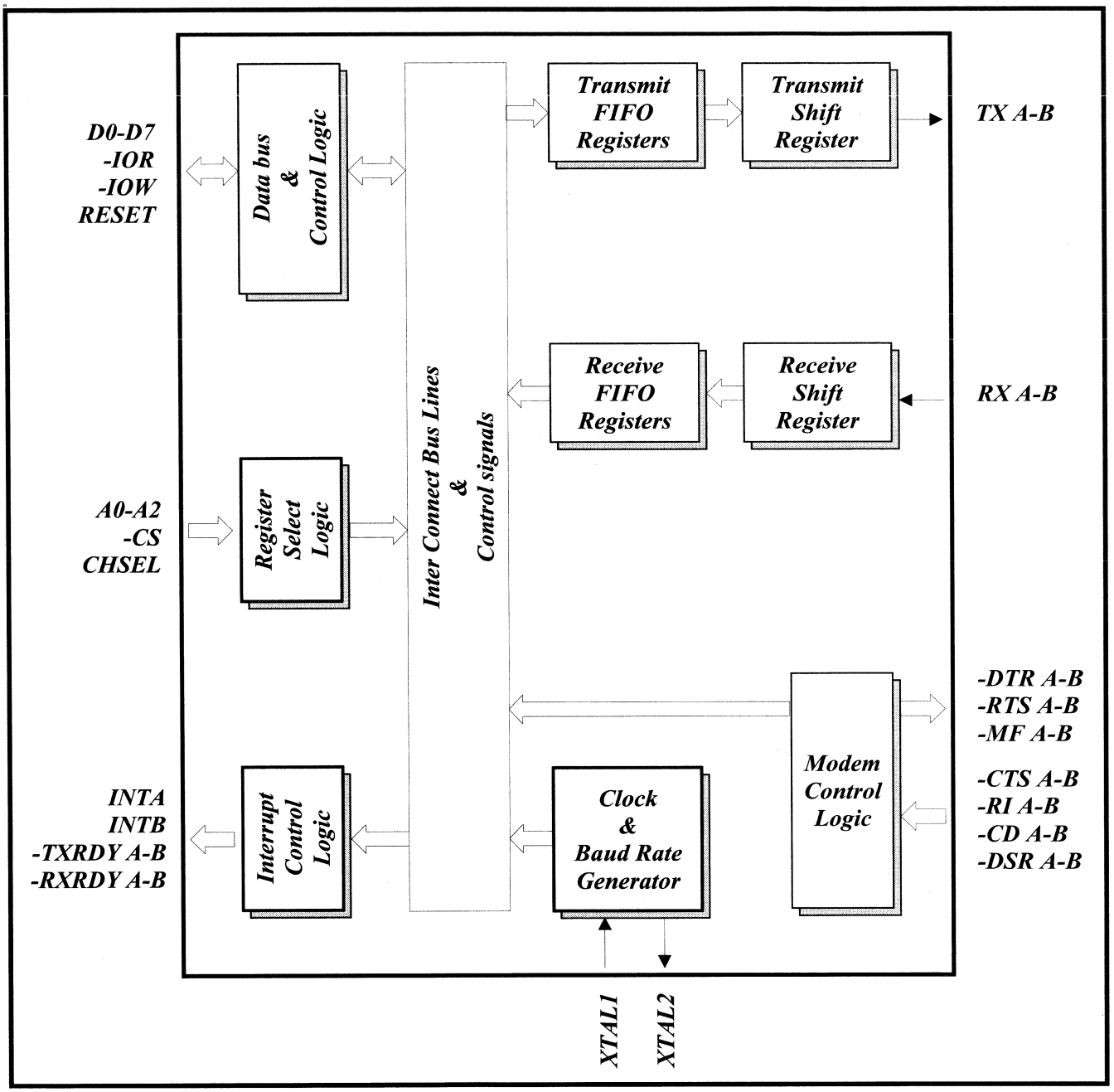
FEATURES

- Pin to pin and functionally compatible to National NS16C552/PC16552
- Software compatible with INS8250, NS16C550/PC16550
- 1.5 Mbps transmit/receive operation (24MHz Max.)
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Independent transmit and receive UART control
- Four selectable Receive FIFO interrupt trigger levels, fixed XMIT FIFO interrupt trigger level
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- DMA operation and DMA monitoring via package I/O pins, TXRDY/RXRDY
- UART internal register sections A & B may be written to concurrently
- Multi function output allows more package functions with fewer I/O pins
- Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C2552CJ44	44-Lead PLCC	0°C to + 70°C
ST16C2552IJ44	44-Lead PLCC	-40°C to + 85°C

BLOCK DIAGRAM



DUAL UART WITH 128-BYTE FIFOs AND RS-485 HALF DUPLEX CONTROL

REV. 1.00

DESCRIPTION

The XR16C2850[1] (2850) is a dual universal asynchronous receiver and transmitter (UART). The 2850 provides enhanced UART functions with 128 byte FIFO, automatic RS-485 half duplex control, a modem control interface, and data rates up to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loopback capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates up to 1.5 Mbps. The baud rate generator can be configured for either crystal or external clock input. The 2850 is available in a 40-pin PDIP, 44-pin PLCC, and 48-pin TQFP packages. The 40 pin package does not offer TXRDY and RXRDY pins (DMA Signal monitoring). Otherwise the three package versions are the same. The 2850 is functionally compatible with the ST16C2550. The 2850 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

1. Covered by U.S. patents #5,649,122, #5,949,787

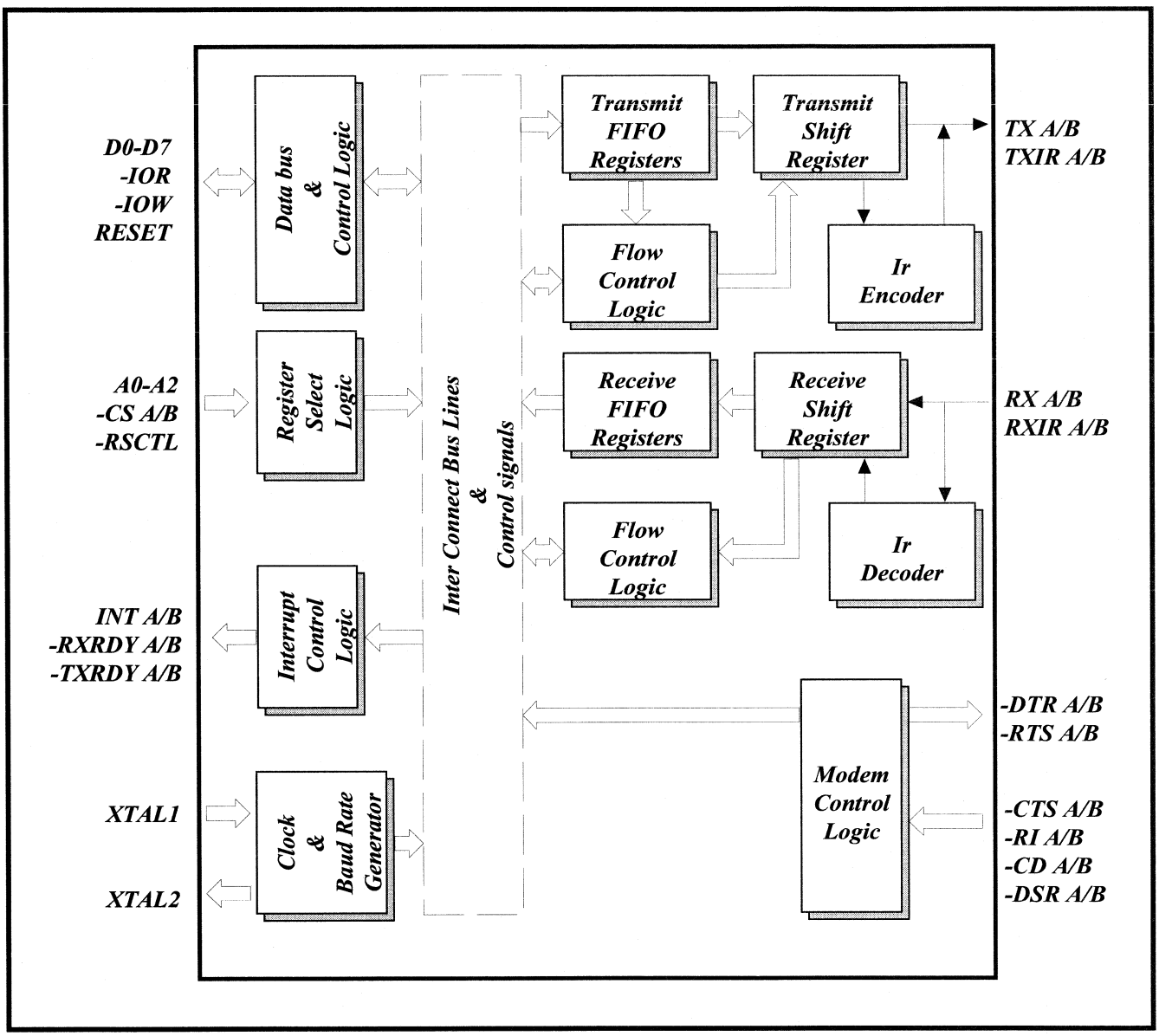
FEATURES

- Pin and functionally compatible to ST16C2550/ TL16C752
- Software compatible with INS8250, NS16C550/ PC16550
- 1.5 Mbps transmit/receive operation (24 MHz Max.)
- 128 byte transmit FIFO to reduce bandwidth requirement of the external CPU
- 128 byte receive FIFO with error flags to reduce bandwidth requirement of the external CPU
- Independent transmit and receive UART control
- RS-485 half duplex enable pin (48-TQFP)
- Programmable transmit/receive FIFO trigger levels
- Hardware/software flow control
- Selectable RTS flow control hysterisis
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD, and software controllable line break)
- Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity
- Infrared receive and transmit encoder/decoder.
- Device identification
- Crystal or external clock input
- +5V or 3.3V operation
- 460.8 Kbps transmit/receive operation with 7.3728 MHz crystal or external clock source

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR16C2850CP	40-Lead PDIP	0°C to + 70°C
XR16C2850CJ	44-Lead PLCC	0°C to + 70°C
XR16C2850CM	48-Lead TQFP	0°C to + 70°C
XR16C2850IP	40-Lead PDIP	-40°C to + 85°C
XR16C2850IJ	44-Lead PLCC	-40°C to + 85°C
XR16C2850IM	48-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



DUAL UART WITH 128-BYTE FIFOs AND RS-485 HALF DUPLEX CONTROL

REV. 1.00

DESCRIPTION

The XR16C2852[1] is a dual universal asynchronous receiver and transmitter (UART). The XR16C2852 provides enhanced UART functions with 128 byte FIFO, automatic RS-485 half duplex control, a modem control interface, and data rates up to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. An alternate function register supports concurrent write to UART A and B. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loopback capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates up to 1.5 Mbps. The baud rate generator can be configured for either crystal or external clock input. The XR16C2852 is available in a 44-pin PLCC package and functionally compatible with the ST16C2552. The XR16C2852 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

1. Covered by U.S. patents #5,649,122, #5,949,787

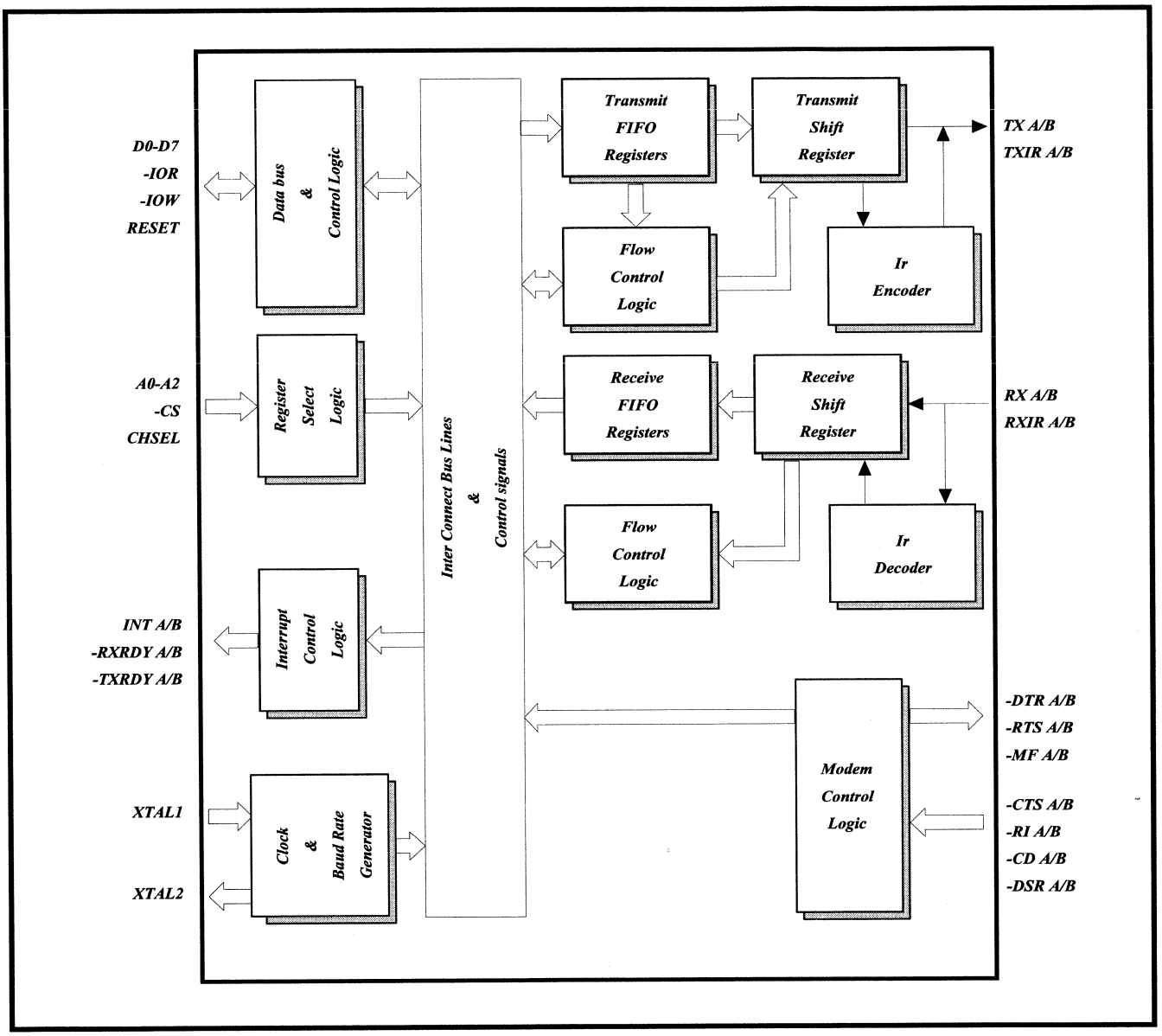
FEATURES

- Pin and functionally compatible to ST16C2552, PC16552
- 1.5 Mbps transmit/receive operation (24 MHz Max.)
- 128 byte transmit FIFO to reduce bandwidth requirement of the external CPU
- 128 byte receive FIFO with error flags to reduce bandwidth requirement of the external CPU
- Independent transmit and receive UART control
- RS-485 half duplex control
- Programmable transmit/receive FIFO trigger levels
- Hardware/software flow control
- Selectable RTS flow control hysterisis
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD, and software controllable line break)
- Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity
- Infrared receive and transmit encoder/decoder
- Device identification
- Crystal or external clock input
- 460.8 Kbps transmit/receive operation with 7.3728 MHz crystal or external clock source
- +5V or 3.3V operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR16C2852CJ	44-Lead PLCC	0°C to + 70°C
XR16C2852IJ	44-Lead PLCC	-40°C to + 85°C

BLOCK DIAGRAM



UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

DESCRIPTION

The ST16C450 is a universal asynchronous receiver and transmitter. The ST16C450 is an improved version of the 16450 UART with higher operating speed and lower access time. A programmable baud rate generator is provided to select transmit and receive clock rates from 50 bps to 1.5 Mbps.

The ST16C450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete modem control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C450 provides internal loopback capability for on board diagnostic testing.

The ST16C450 is available in 40 pin PDIP, 44 pin PLCC and 48 pin TQFP packages. It is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

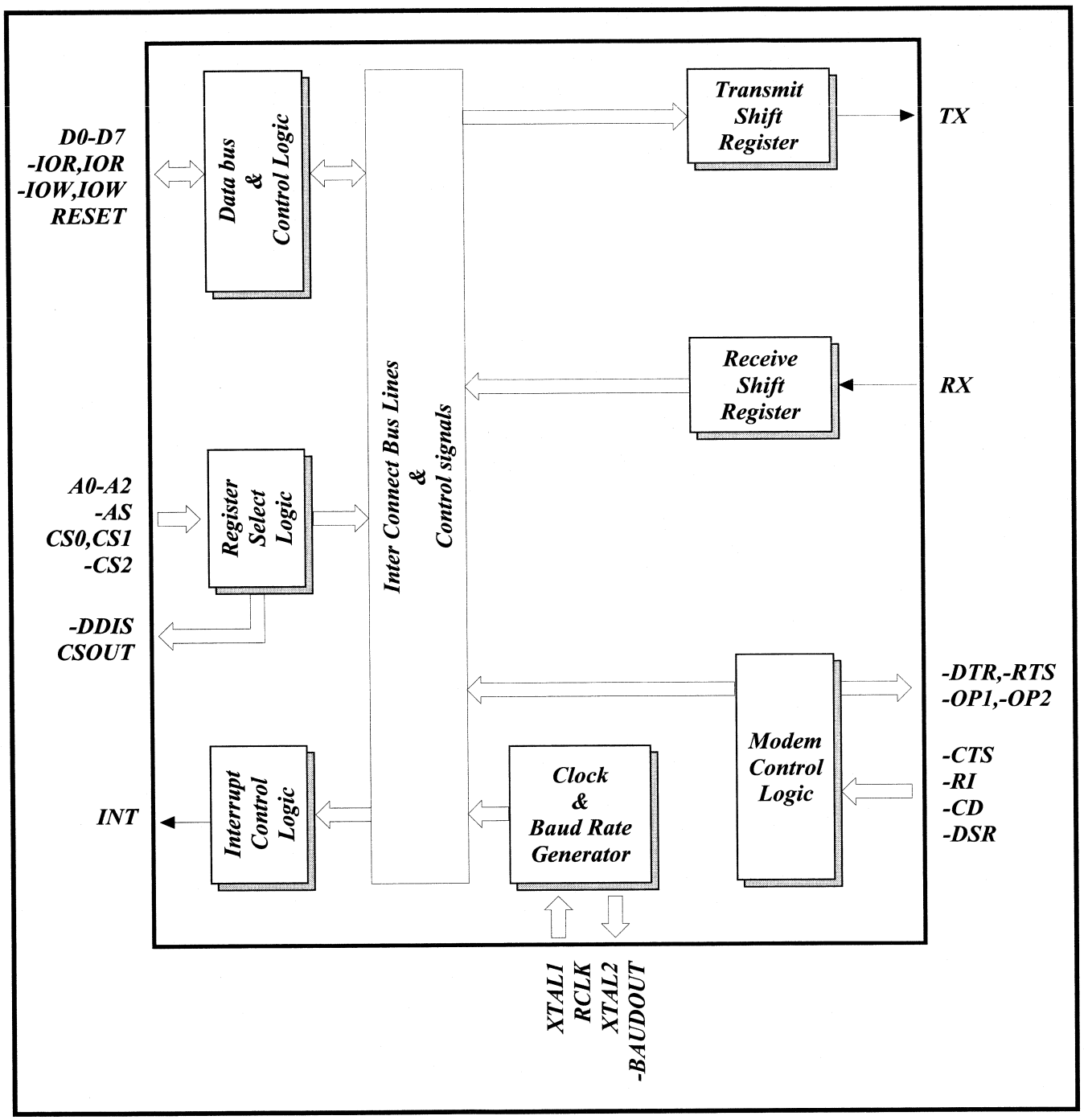
FEATURES

- Pin to pin and functionally compatible to the Industry Standard 16450
- 1.5 Mbps transmit/receive operation (24MHz)
- Programmable word lengths (5, 6, 7, 8)
- Even, odd, force, or no parity generation and detection
- Independent transmit and receive control
- Standard modem interface
- Low operating current (1.2mA typ.)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C450CP40	40-Lead PDIP	0°C to +70°C
ST16C450CJ44	44-Lead PLCC	0°C to +70°C
ST16C450CQ48	48-Lead TQFP	0°C to +70°C
ST16C450IP40	40-Lead PDIP	-40°C to +85°C
ST16C450IJ44	44-Lead PLCC	-40°C to +85°C
ST16C450IQ48	48-Lead TQFP	-40°C to +85°C

BLOCK DIAGRAM



DUAL UART WITH PARALLEL PRINTER PORT

DESCRIPTION

The ST16C452/ST16C452PS (452/452PS) is a dual universal asynchronous receiver and transmitter (UART) with an added bi-directional parallel port that is directly compatible with a CENTRONICS type printer. The parallel port is designed such that the user can configure it as general purpose I/O interface, or for connection to other printer devices. The 452/452PS provides enhanced UART functions, a modem control interface, and data rates up to 1.5Mbps. On-board status registers provide the user with error indications and operational status. The system interrupts and control may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. A programmable baud rate generator is provided to select transmit and receive clock rates from 50 bps to 1.5 Mbps. The 452/452PS is available in a 68 pin PLCC package. The 452/452PS is compatible with the 16C450. The 452 is available in two versions, the ST16C452 and the ST16C452PS. The ST16C452 provides single hardware pin to control the printer port data direction while the 452PS provides an additional software control bit to control the printer port data direction to become compatible PS/2 operating system.

The 452/452PS is fabricated in an advanced CMOS process with low power consumption.

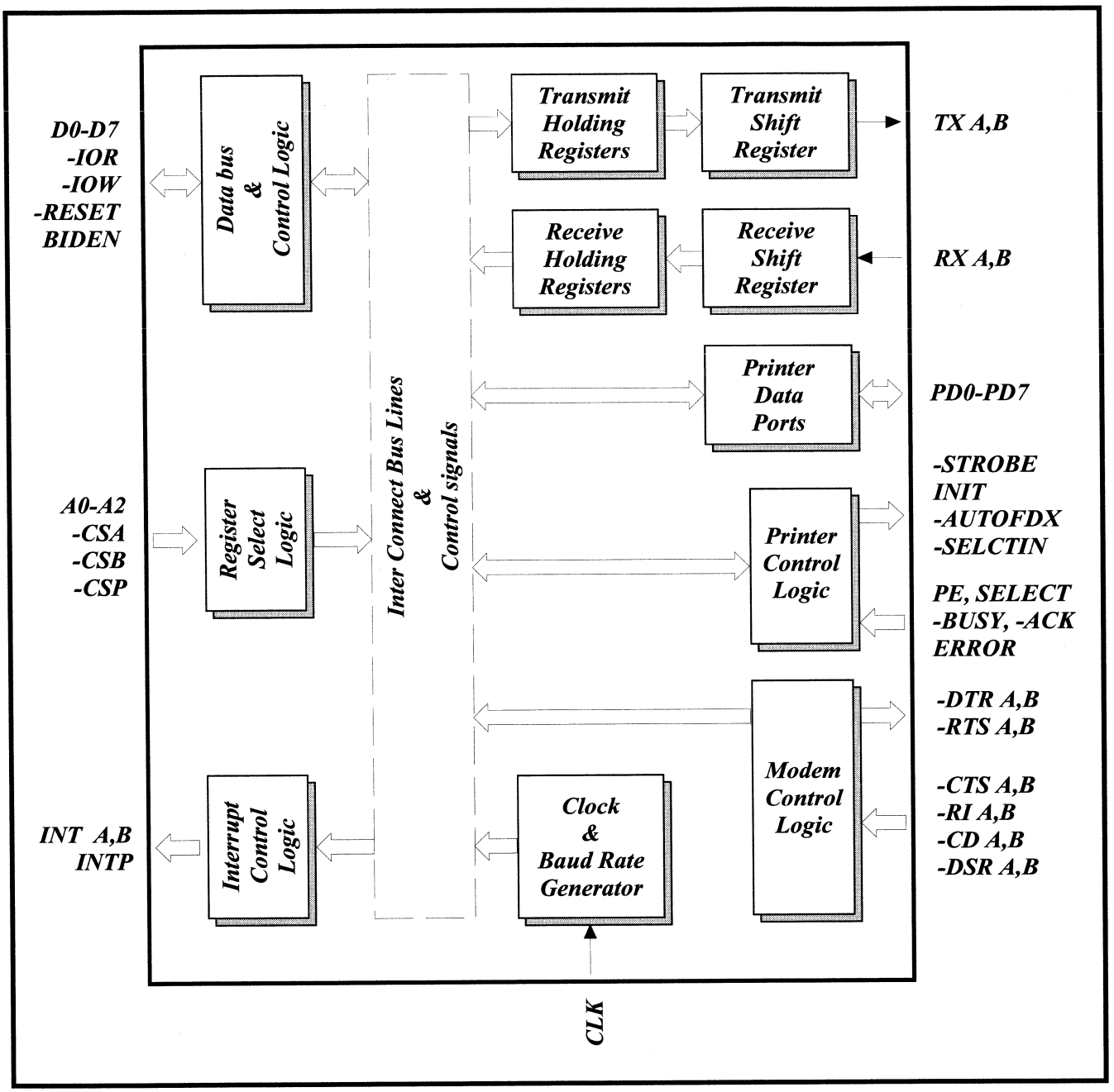
FEATURES

- Pin to pin and functional compatible to TL16C452
- Software compatible with ST16C450, 16C450
- 1.5 Mbps transmit/receive operation (24MHz)
- Independent transmit and receive control
- Modem and printer status registers
- UART port and printer port bi-directional
- Printer port direction set by single control bit or 8 bit pattern (AA/55)
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Internal loop-back diagnostics
- TTL compatible inputs, outputs
- Low Power

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C452CJ68	68-Lead PLCC	0°C to + 70°C
ST16C452CJ68PS	68-Lead PLCC	0°C to + 70°C
ST16C452IJ68	68-Lead PLCC	-40°C to + 85°C
ST16C452IJ68PS	68-Lead PLCC	-40°C to + 85°C

BLOCK DIAGRAM



QUAD UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

REV. 3.20

DESCRIPTION

The ST16C454 (454) is a universal asynchronous receiver and transmitter (UART) with a dual foot print interface. The 454 is an enhanced UART with data rates up to 1.5Mbps and software compatible to ST16C450. Onboard status registers provide the user with error indications and operational status, modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. The ST16C454 offer an additional 68 mode which allows easy integration with Motorola, and other popular microprocessors. The 454 combines the package interface modes of the ST16C454 and ST68C454 series on a single integrated chip.

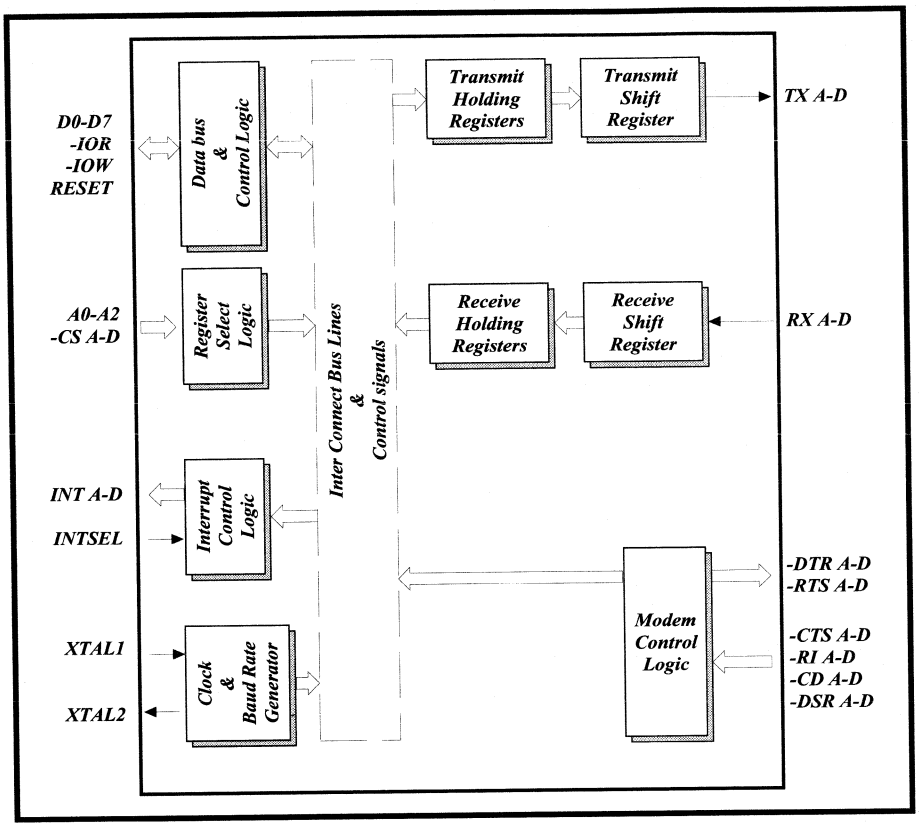
FEATURES

- Software compatibility with the Industry Standard 16C450
- 1.5 Mbps transmit/receive operation (24MHz)
- Independent transmit and receive control
- Software selectable Baud Rate Generator
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Internal loop-back diagnostics
- TTL compatible inputs, outputs
- Low power

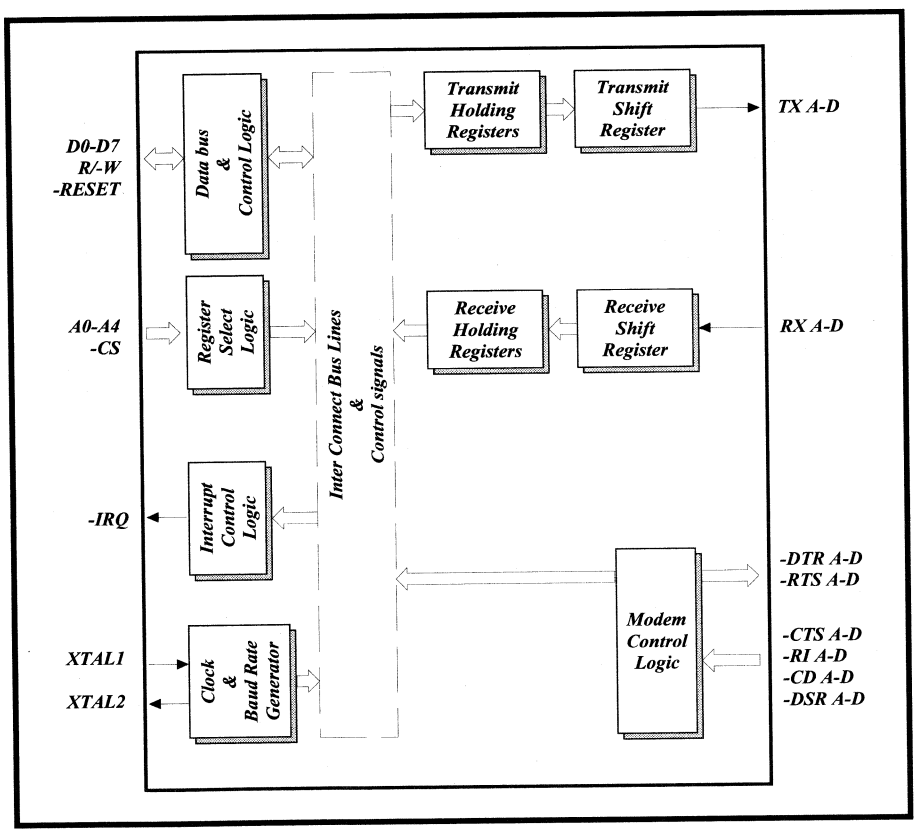
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C454CJ68	68-Lead PLCC	0°C to +70°C
ST16C454IJ68	68-Lead PLCC	-40°C to +85°C
ST68C454CJ68	68-Lead PLCC	0°C to +70°C
ST68C454IJ68	68-Lead PLCC	-40°C to +85°C

BLOCK DIAGRAM 16 MODE



BLOCK DIAGRAM 68 MODE



DESCRIPTION

The ST16C550 (550) is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. It operates at 3.3 and 5V power supplies. A programmable baud rate generator can select transmit and receive clock rates from 50 bps to 1.5 Mbps.

The ST16C550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C550 provides internal loop-back capability for on board diagnostic testing.

The ST16C550 is available in 40 pin PDIP, 44 pin PLCC, and 48 pin TQFP packages. It is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

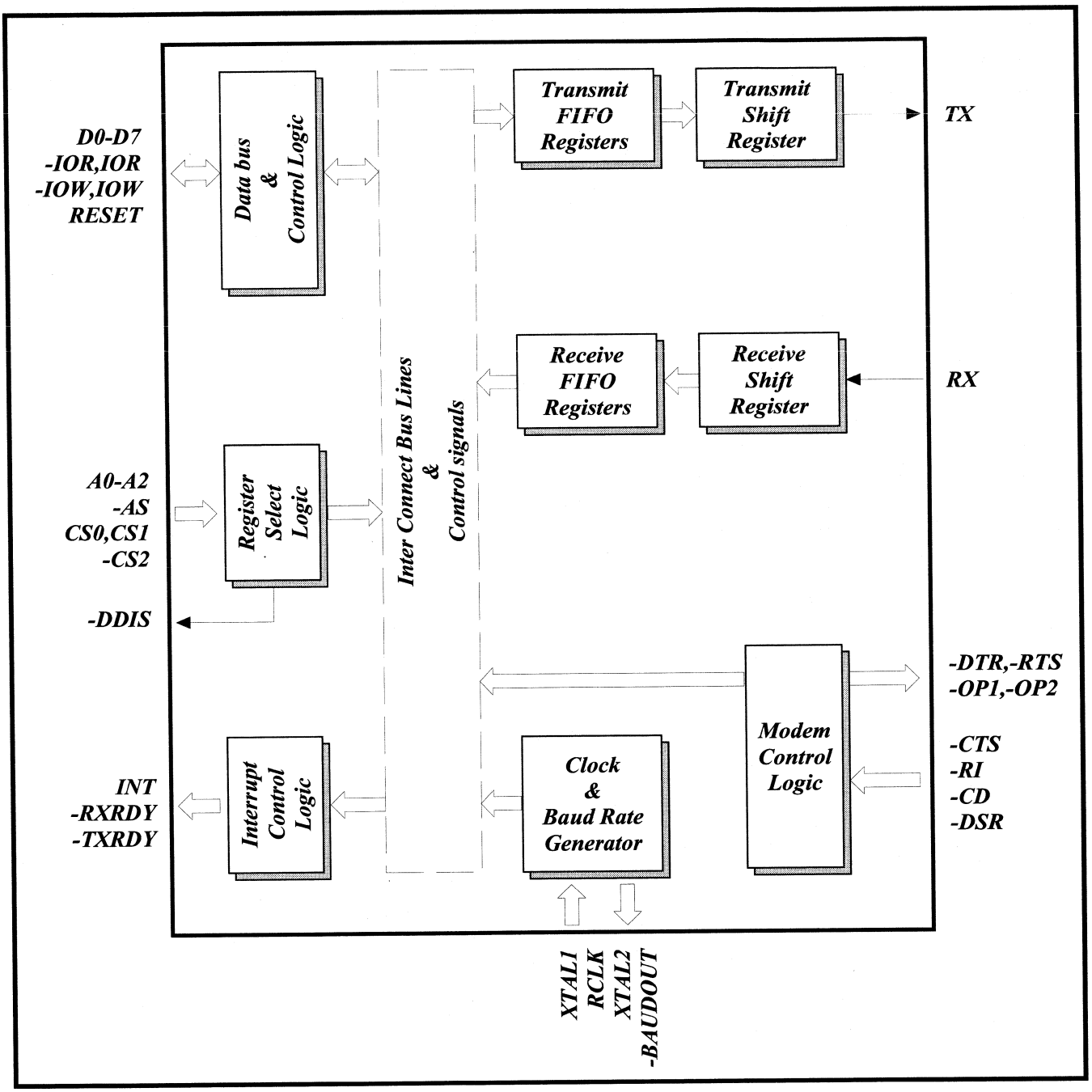
FEATURES

- Pin-to-pin and functionally compatible to the Industry Standard 16C550
- 24MHz clock operation at 5V
- 1.0 Mbps data rate operation at 3.3V
- 16MHz clock operation at 3.3V
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Full duplex operation
- Transmit and receive control
- Four selectable receive FIFO interrupt trigger levels
- Standard modem interface
- Compatible with ST16C450
- Low operating current (1.2mA typ.)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
ST16C550CP40	40-Lead PDIP	0°C to +70°C
ST16C550CJ44	44-Lead PLCC	0°C to +70°C
ST16C550CQ48	48-Lead TQFP	0°C to +70°C
ST16C550IP40	40-Lead PDIP	-40°C to +85°C
ST16C550IJ44	44-Lead PLCC	-40°C to +85°C
ST16C550IQ48	48-Lead TQFP	-40°C to +85°C

ST16C550 BLOCK DIAGRAM



DUAL UART WITH 16-BYTE FIFO AND PARALLEL PRINTER PORT

DESCRIPTION

The ST16C552/ST16C552A (552/552A) is a dual universal asynchronous receiver and transmitter (UART) with an added bi-directional parallel port that is directly compatible with a CENTRONICS type printer. The parallel port is designed such that the user can configure it as general purpose I/O interface, or for connection to other printer devices. The 552/552A provides enhanced UART functions with 16 byte FIFO's, a modem control interface, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status. The system interrupts and control may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. A programmable baud rate generator is provided to select transmit and receive clock rates from 50 bps to 1.5 Mbps. The 552/552A is available in a 68 pin PLCC package. The 552/552A is compatible with the 16C450 and 16C550. The difference between the ST16C552 and ST16C552A is the logic state of the printer port, INTP interrupt. The INTP interrupt is active high (logic 1) on the ST16C552 whereas INTP is active low (logic 0) on the ST16C552A part, when the interrupt latch mode is selected. The 552/552A is fabricated in an advanced CMOS process with power down mode to reduce the power consumption. The 552A does not support the power down mode.

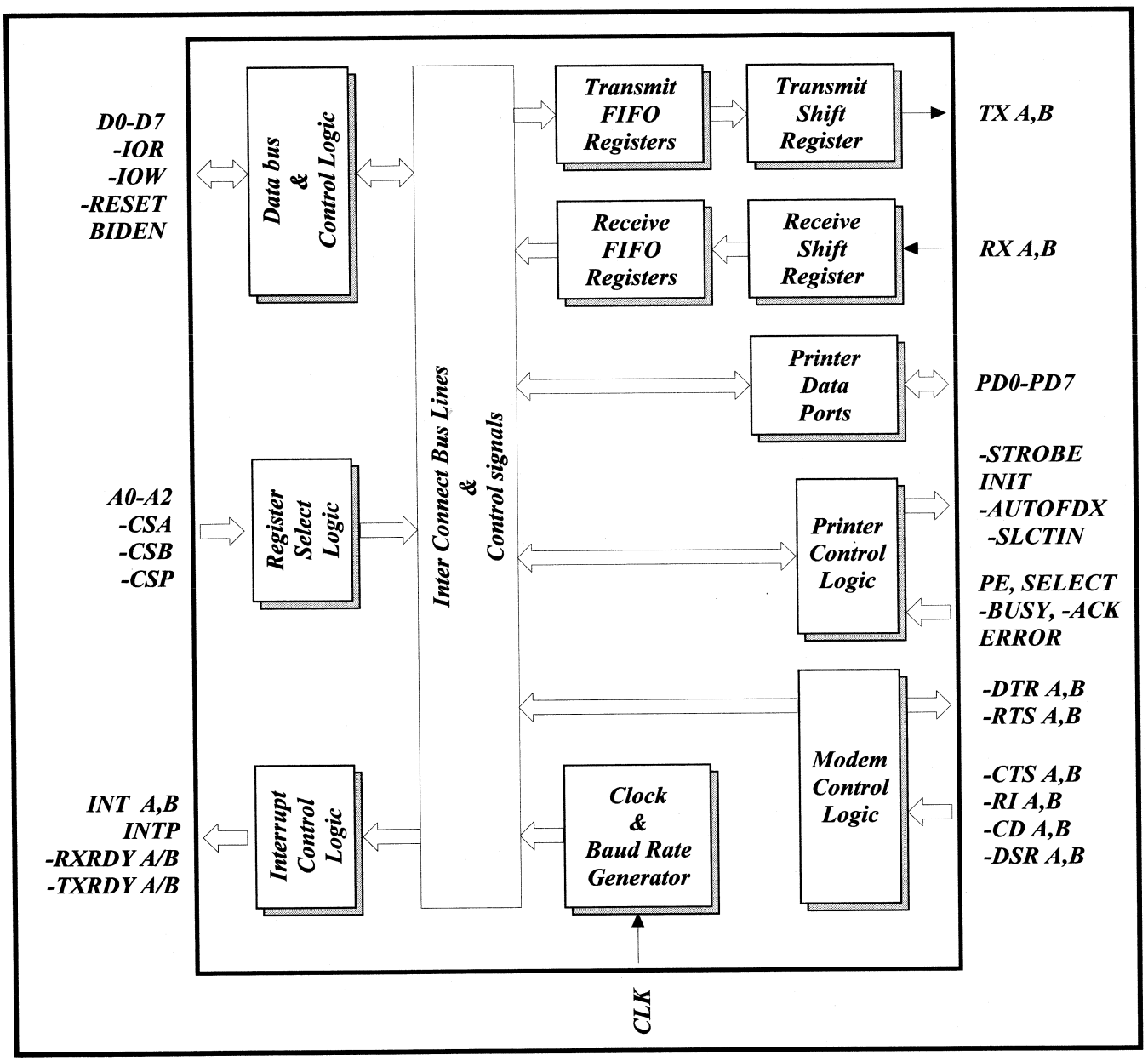
FEATURES

- Pin to pin and functional compatible to ST16C452/452PS, TL16C552A
- Software compatible with INS8250, NS16C550/PC16550
- 1.5 Mbps transmit/receive operation (24MHz)
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Independent transmit and receive control
- Modem and printer status registers
- UART port and printer port bi-directional
- Printer port direction set by single control bit or 8 bit pattern (AA/55)
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Internal loop-back diagnostics
- TTL compatible inputs, outputs
- Power down mode

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C552CJ68	68-Lead PLCC	0°C to + 70°C
ST16C552ACJ68	68-Lead PLCC	0°C to + 70°C
ST16C552IJ68	68-Lead PLCC	-40°C to + 85°C
ST16C552AIJ68	68-Lead PLCC	-40°C to + 85°C

BLOCK DIAGRAM



QUAD UART WITH 16-BYTE FIFOs

DESCRIPTION

The ST16C554D is a universal asynchronous receiver and transmitter (UART) with a dual foot print interface. The 554D is an enhanced UART with 16 byte FIFOs, receive trigger levels and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status, modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows onboard diagnostics. The 554D is available in 64 pin TQFP, and 68 pin PLCC packages. The 68 pin PLCC package offer an additional 68 mode which allows easy integration with Motorola, and other popular microprocessors. The ST16C554CQ64 (64 pin) offers three state interrupt control while the ST16C554DCQ64 provides constant active interrupt outputs. The 64 pin devices do not offer TXRDY/RXRDY outputs. The 554D combines the package interface modes of the 16C554 and 68C554 series on a single integrated chip.

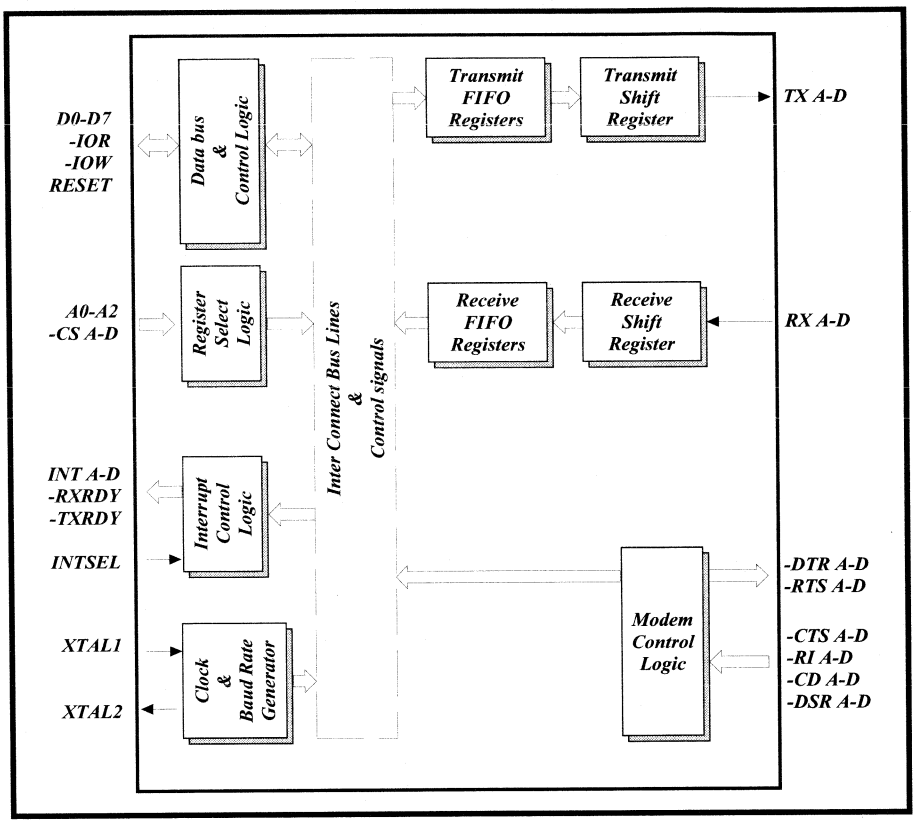
FEATURES

- Compatibility with the Industry Standard ST16C454, ST68C454, ST68C554
- ST16C554 is compatible to TL16C554
- 1.5 Mbps transmit/receive operation (24MHz)
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Independent transmit and receive control
- Software selectable Baud Rate Generator
- Four selectable Receive FIFO interrupt trigger levels
- Standard modem interface

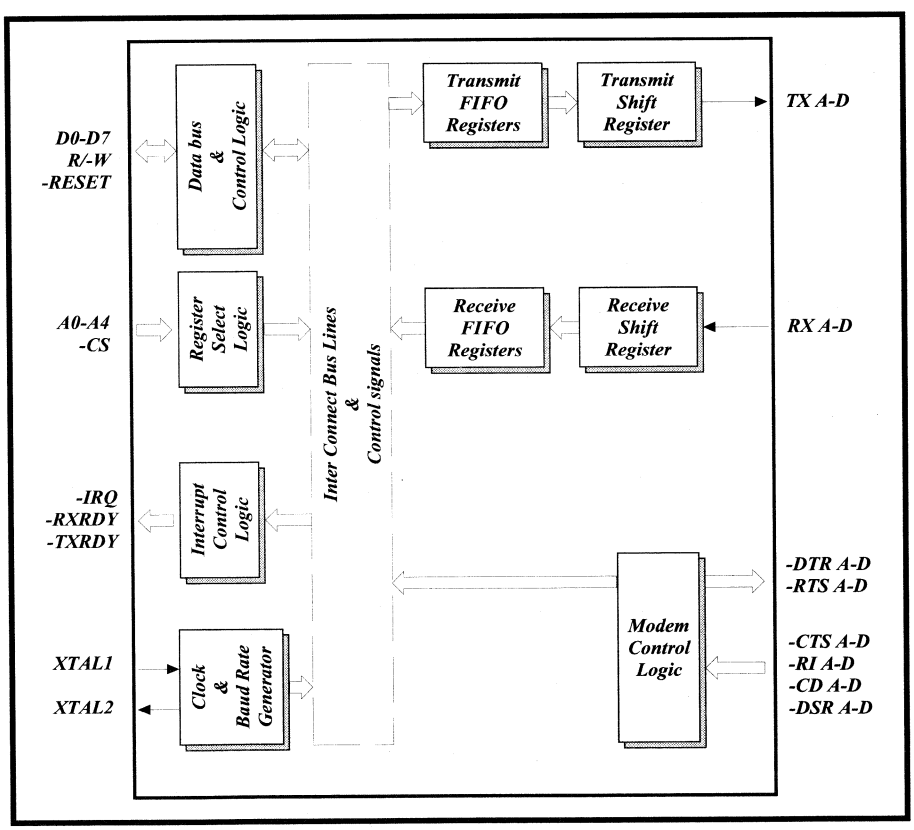
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C554DCJ68	68-Lead PLCC	0°C to + 70°C
ST16C554DCQ64	64-Lead TQFP	0°C to + 70°C
ST16C554CQ64	64-Lead TQFP	0°C to + 70°C
ST16C554DIJ68	68-Lead PLCC	-40°C to + 85°C
ST16C554DIQ64	64-Lead TQFP	-40°C to + 85°C
ST68C554CJ68	68-Lead PLCC	0°C to + 70°C
ST68C554IJ68	68-Lead PLCC	-40°C to + 85°

BLOCK DIAGRAM 16 MODE



BLOCK DIAGRAM 68 MODE



UART WITH 16-BYTE FIFOs AND INFRARED (IRDA) ENCODER/DECODER

GENERAL DESCRIPTION

The ST16C580[1] is a universal asynchronous receiver and transmitter (UART) and is pin compatible with the ST16C550 UART. The ST16C580 is an enhanced UART with 16 byte FIFO's, automatic hardware/software flow control, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status. Modem interface control is included and can be optionally configured to operate with the Infrared (IrDA) encoder/decoder. The system interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. The ST16C580 is available in 40 pin PDIP, 44 pin PLCC and 48 pin TQFP packages. It is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

1. Covered by U.S. patent #5,643,122.

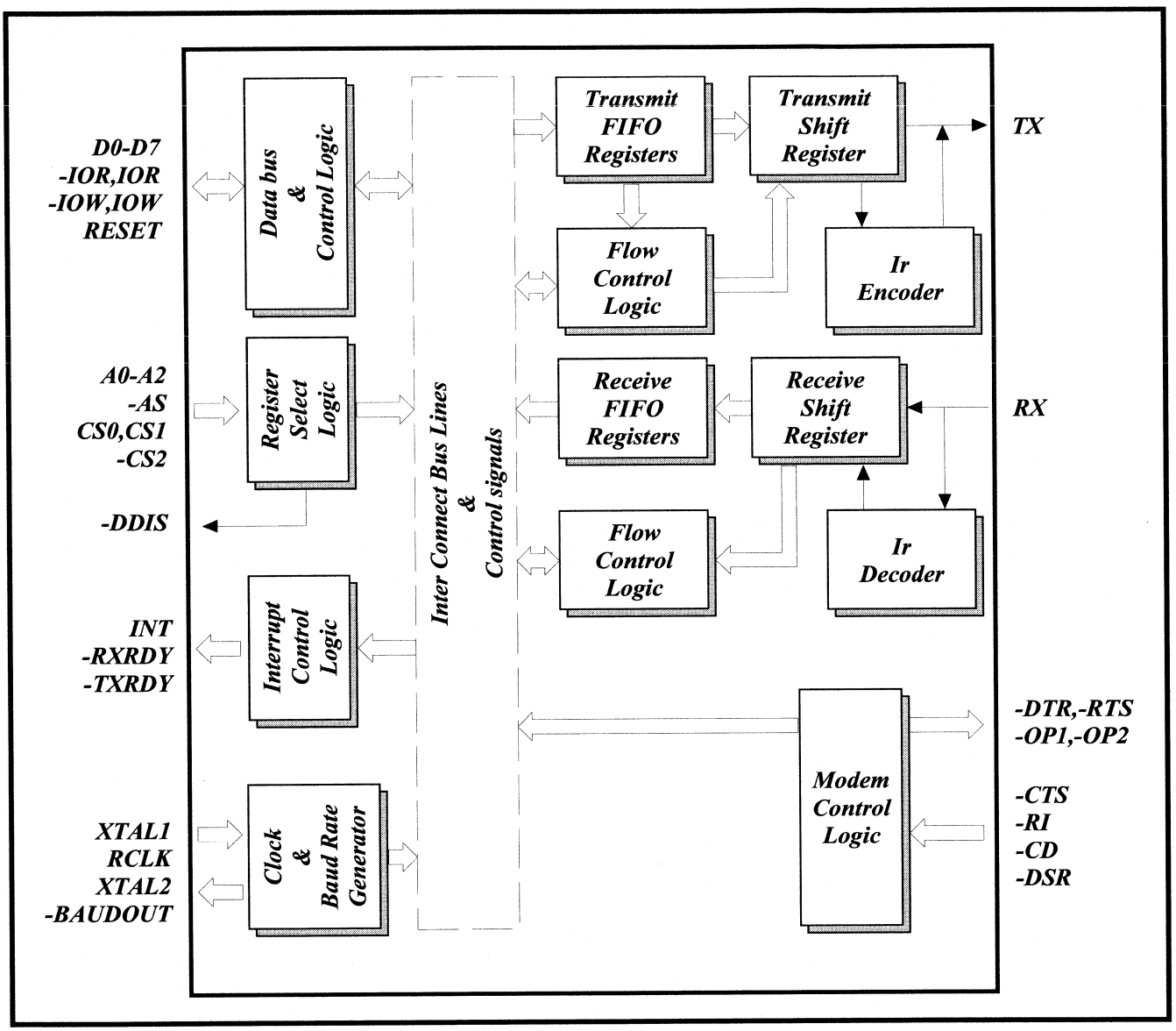
FEATURES

- Pin to pin and functionally compatible to the Industry Standard 16550
- 1.5 Mbps transmit/receive operation (24MHz)
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Automatic hardware/software flow control
- Programmable Xon/Xoff characters
- Independent transmit and receive control
- Software selectable Baud Rate Generator pre-scaleable clock rates of 1X or 4X
- Four selectable transmit/receive FIFO interrupt trigger levels
- Standard modem interface or Infrared IrDA encode/decoder interface
- Sleep mode (200µA stand-by)
- Low operating current (1.2mA typ.)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C580CP40	40-Lead PDIP	0°C to + 70°C
ST16C580CJ44	44-Lead PLCC	0°C to + 70°C
ST16C580CQ48	48-Lead TQFP	0°C to + 70°C
ST16C580IP40	40-Lead PDIP	-40°C to + 85°C
ST16C580IJ44	44-Lead PLCC	-40°C to + 85°C
ST16C580IQ48	48-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



UART WITH 32-BYTE FIFOs AND INFRARED (IRDA) ENCODER/DECODER

GENERAL DESCRIPTION

The ST16C650A[1] is a universal asynchronous receiver and transmitter (UART) with 5V tolernat inputs. It is pin compatible with the ST16C450/550/650 UART. The 650A is an enhanced UART with 32 byte of transmit and receive FIFOs, automatic hardware/software flow control, data rates up to 3 Mbps and automatic RS485 direction control for half-duplex operation. Onboard status registers provide the user with error indications and operational status. Modem interface control is included and can be optionally configured to operate with the Infrared (IrDA) encoder/decoder. The system interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. The 650A supports 2 bus interface, standard (STD) and PC ISA (PC) mode. The STD mode is compatible with the ST16C450, ST16C550 and ST16C650 while the PC mode allows direct interfacing to the PC ISA bus.The 650A is available in 48 pin TQFP, 44 pin PLCC and 40 pin PDIP packages. The 44 and 48 pin packages support the STD or PC mode. The 40 pin package supports only the STD mode.

1. Covered by U.S. patent #5,643,122.

FEATURES

Added features in device revision "H" and newer:

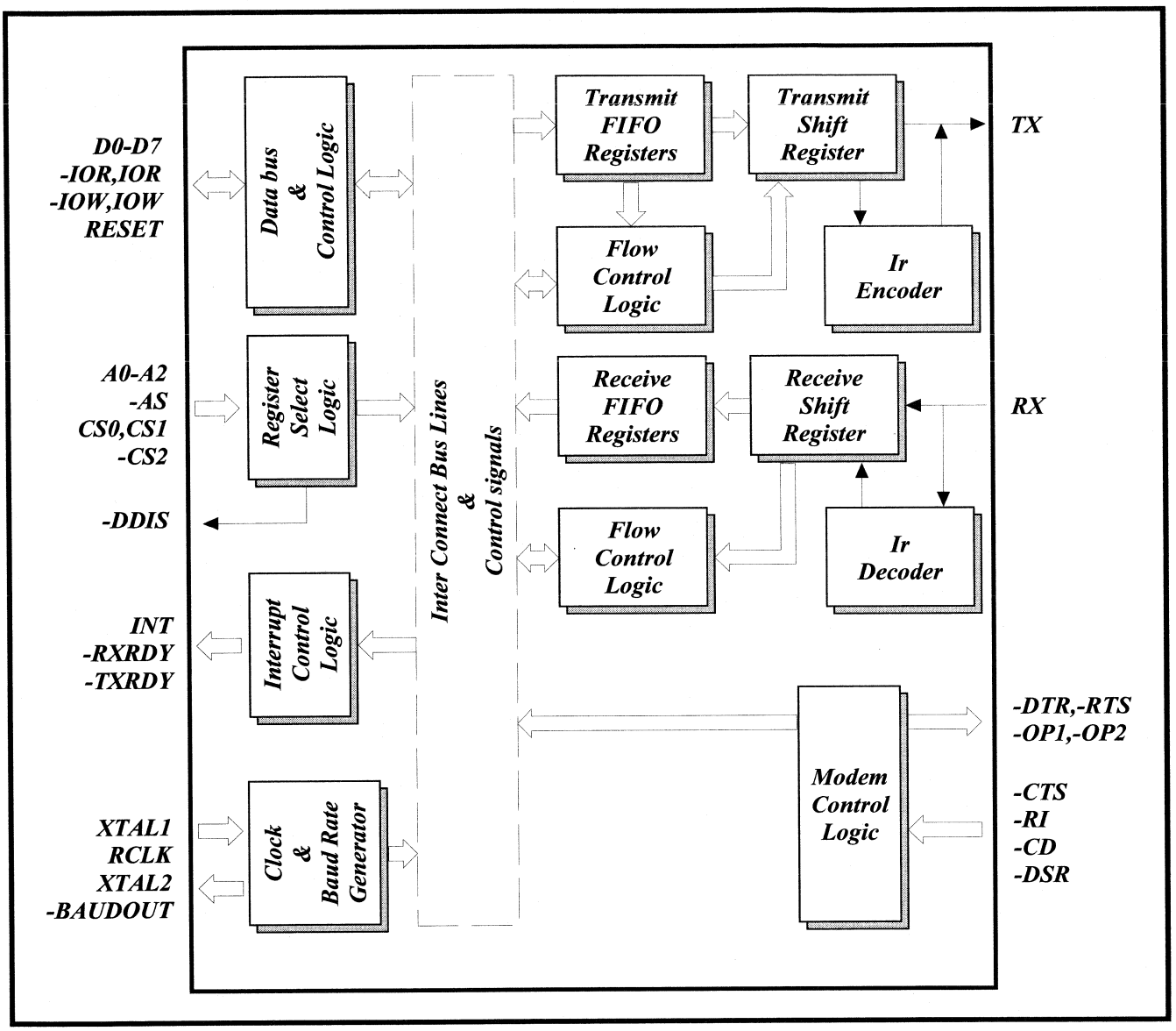
- 2.90V to 5.5V Operation
- 5V Tolerant Inputs
- 3 Mbps data rate at 5V and 2 Mbps at 3.3V
- Auto RS485 Half-duplex control output
- Wireless Infrared (IrDA) encoder with program mable pulse width capability and decoder interface
- Device Identification & Revision Codes
- Sleep mode with wake-up indicator

- Pin to pin and functionally compatible to the Industry Standard 16C550
- 32 byte transmit FIFO
- 32 byte receive FIFO with error flags
- Automatic hardware/software flow control
- Programmable Xon/Xoff characters
- Independent transmit and receive control
- Software selectable Baud Rate Generator prescaleable clock rates of 1X or 4X
- Four selectable transmit/receive FIFO interrupt trigger levels
- STD mode is compatible with ST16C450/550/650
- PC mode provides PC ISA bus COM and LPT port address decoding

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C650ACP40	40-Lead PDIP	0°C to + 70°C
ST16C650ACJ44	44-Lead PLCC	0°C to + 70°C
ST16C650ACQ48	48-Lead TQFP	0°C to + 70°C
ST16C650AIP40	40-Lead PDIP	-40°C to + 85°C
ST16C650AIJ44	44-Lead PLCC	-40°C to + 85°C
ST16C650AIQ48	48-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



QUAD UART WITH 64-BYTE FIFO AND INFRARED (IRDA) ENCODER/DECODER

DESCRIPTION

The ST16C654 is a universal asynchronous receiver and transmitter (UART) with a dual foot print interface compatible with the ST16C554 and ST68C554. The 654 is an enhanced UART with 64 byte FIFO's, automatic hardware/software flow control, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status, modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows onboard diagnostics. The 654 is available in 64 pin TQFP, 68 pin PLCC, and 100 pin QFP packages. The 64 pin package offers the 16 interface mode which is compatible with the industry standard ST16C554. The 68 and 100 pin packages offer an additional 68 mode which allows easy integration with Motorola, and other popular microprocessors. The ST16C654CQ64 (64 pin) offers three state interrupt control while the ST16C654DCQ64 provides constant active interrupt outputs. The 64 pin devices do not offer TXRDY/RXRDY outputs or the default clock select option (CLKSEL). The 100 pin packages offer faster channel status access by providing separate outputs for TXRDY and RXRDY, offer separate Infrared TX outputs and a musical instrument clock input (MIDICLK). The 654 combines the package interface modes of the 16C454/554 and 68/C454/554 series on a single integrated chip.

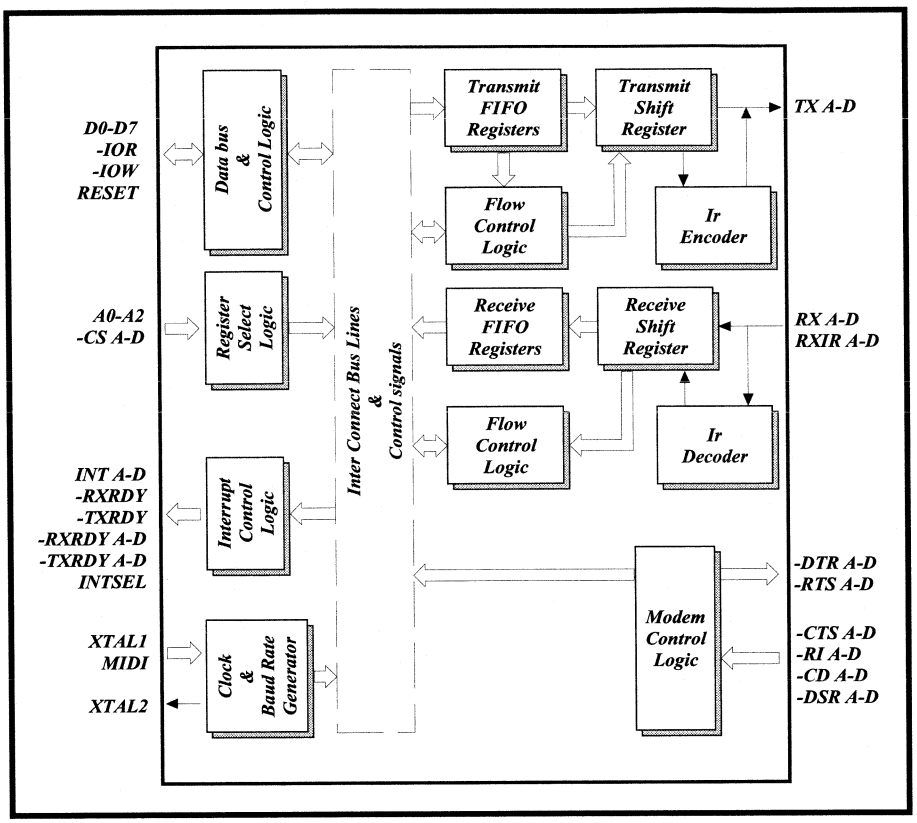
FEATURES

- Compatibility with the Industry Standard ST16C454/554, ST68C454/554
- ST16C654 is compatible to TL16C554
- 1.5 Mbps transmit/receive operation (24MHz)
- 64 byte transmit FIFO
- 64 byte receive FIFO with error flags
- Automatic software/hardware flow control
- Programmable Xon/Xoff characters
- Independent transmit and receive control
- Software selectable Baud Rate Generator prescaleable clock rates of 1x, 4x.
- Four selectable Transmit/Receive FIFO interrupt trigger levels
- Standard modem interface or infrared IrDA encoder/decoder interface
- Software flow control turned off optionally by any (Xon) Rx character
- Independent MIDI interface on 100 pin packages
- 100 pin packages offer internal register FIFO monitoring and separate IrDA Tx outputs
- Sleep mode (200mA stand-by)

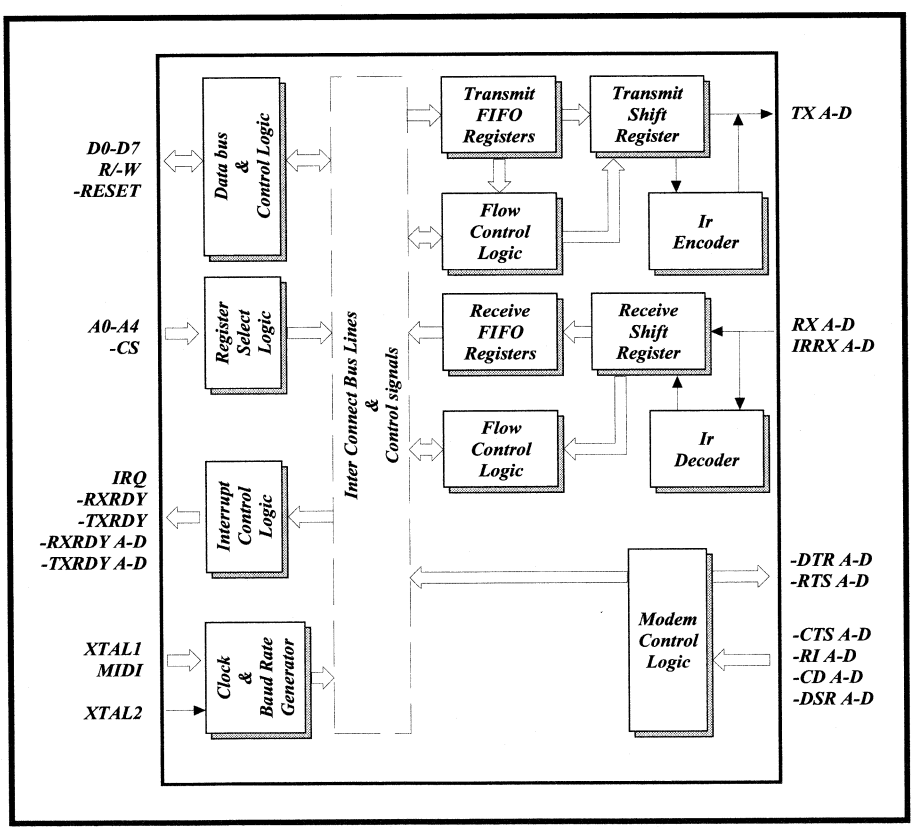
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
ST16C654CJ68	68-Lead PLCC	0°C to + 70°C
ST16C654CQ64	64-Lead TQFP	0°C to + 70°C
ST16C654DCQ64	64-Lead TQFP	0°C to + 70°C
ST16C654CQ100	100-Lead QFP	0°C to + 70°C
ST16C654IJ68	68-Lead PLCC	-40°C to + 85°C
ST16C654IQ64	64-Lead TQFP	-40°C to + 85°C
ST16C654DIQ64	64-Lead TQFP	-40°C to + 85°C
ST16C654CQ100	100-Lead QFP	-40°C to + 85°C

BLOCK DIAGRAM 16 MODE



BLOCK DIAGRAM 68 MODE



DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

REV. 2.10

DESCRIPTION

The EXAR Dual Universal Asynchronous Receiver and Transmitter (DUART) is a data communications device that provides two fully independent full duplex asynchronous communications channels in a single package. The DUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

The XR68C681 device offers a single IC solution for the 68000 family of microprocessors

The DUART is fabricated using advanced CMOS process to provide high performance and low power consumption, and is packaged in a 40 pin DIP or a 44 pin PLCC.

FEATURES

- Two Full Duplex, Independent Channels
- Asynchronous Receiver and Transmitter
- Quadruple-Buffered Receiver, Dual Buffered Transmitter
- Programmable Stop Bits in 1/16 Bit Increments
- Internal Bit Rate Generators with 23 Different Bit Rates
- Independent Bit Rate Selection for Each Transmitter and Receiver
- External Clock Capability
- Maximum Bit Rate: 1X Clock - 1Mb/s, 16X Clock - 125Kb/s
- Normal, AUTOECHO, Local LOOPBACK and
- Remote LOOPBACK Modes
- Multi-function 16 Bit Counter/Timer
- Interrupt Output with Eight Maskable Interrupt Conditions
- Interrupt Vector Output on Acknowledge
- 8 General Purpose Outputs
- 6 General Purpose Inputs with Change of States Detectors on Inputs
- On-chip Oscillator for Crystal
- Standby Mode to Reduce Operating Power
- Pin Compatible with the Motorola MC68681 and the Philips SCC68692 Devices
- Advanced CMOS Low Power Technology

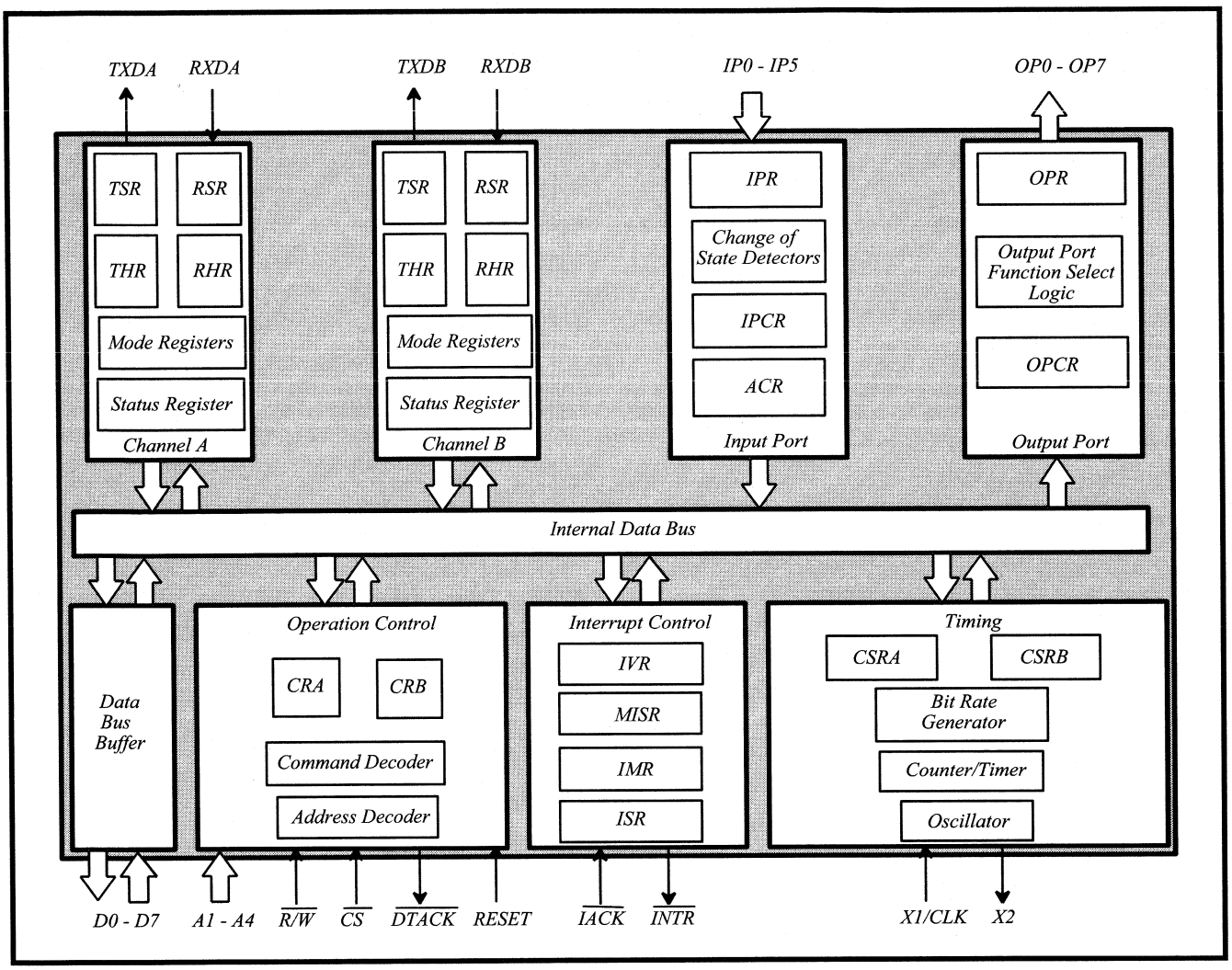
APPLICATIONS

- Multimedia Systems
- Serial to Parallel/Parallel to Serial Converter
- DTE for Modem Communication Systems

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR68C681CJ	44-Lead PLCC	0°C to + 70°C
XR68C681CP	40-Lead PDIP	0°C to + 70°C
XR68C681P	40-Lead PDIP	-40°C to + 85°C
XR68C681J	44-Lead PLCC	-40°C to + 85°C
XR68C681N	40-Lead CDIP	-40°C to + 85°C

BLOCK DIAGRAM



DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

REV. 2.01

DESCRIPTION

The EXAR Dual Universal Asynchronous Receiver and Transmitter (DUART) is a data communications device that provides two fully independent full duplex asynchronous communication channels in a single package. The DUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

The XR88C681 device offers a single IC solution for the 8080/85, 8086/88, Z80, Z8000, 68xx and 65xx microprocessor families.

The DUART is fabricated using advanced CMOS process to provide high performance and low power consumption, and is packaged in a 40 pin PDIP, a 28 pin PDIP, and a 44 pin PLCC.

FEATURES

- Two Full Duplex, Independent Channels
- Asynchronous Receiver and Transmitter
- Quadruple-Buffered Receivers and Dual Buffered Transmitters
- Programmable Stop Bits in 1/16 Bit Increments
- Internal Bit Rate Generators with More than 23 Bit Rates
- Independent Bit Rate Selection for Each Transmitter and Receiver
- External Clock Capability
- Maximum Bit Rate: 1X Clock - 1Mb/s, 16X Clock - 125kb/s
- Normal, AUTOECHO, Local LOOPBACK and Remote LOOPBACK Modes
- Multi-function 16 Bit Counter/Timer
- Interrupt Output with Eight Maskable Interrupt Conditions
- Interrupt Vector Output on Acknowledge (40 Pin DIP and 44 Pin PLCC Packages Only)
- Programmable Interrupt Daisy Chain
- 8 General Purpose Outputs (40 Pin DIP and 44 Pin PLCC Packages Only)
- 7 General Purpose Inputs with Change of States Detectors on Inputs (40 Pin DIP and 44 Pin PLCC Packages Only)
- Multi-Drop Mode Compatible with 8051 Nine Bit Mode
- On-Chip Oscillator for Crystal
- Standby Mode to Reduce Operating Power
- Pin Compatible with the Motorola MC2681 and Philips SCC2692 devices
- Advanced CMOS Low Power Technology

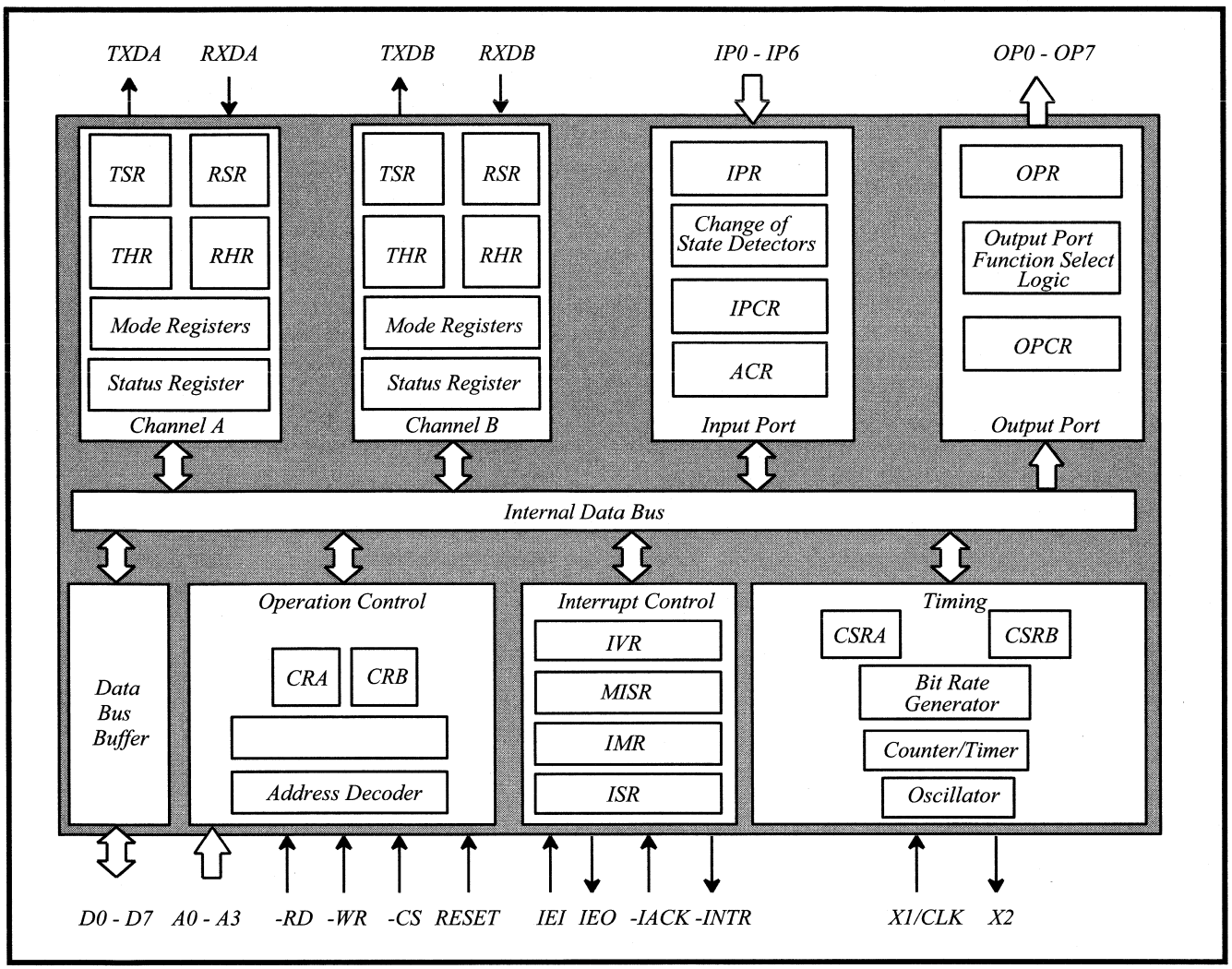
APPLICATIONS

- Multimedia Systems
- Serial to Parallel/Parallel to Serial Converter
- DTE for Modem Communication Systems

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR88C681CJ44	44-Lead PLCC	0°C to + 70°C
XR88C681CP28	28-Lead PDIP	0°C to + 70°C
XR88C681CP40	40-Lead PDIP	0°C to + 70°C
XR88C681P28	28-Lead PDIP	-40°C to + 85°C
XR88C681P40	40-Lead PDIP	-40°C to + 85°C
XR88C681J	44-Lead PLCC	-40°C to + 85°C
XR88C681N40	40-Lead CDIP	-40°C to + 85°C
XR88C681CN40	40-Lead CDIP	0°C to + 70°C

BLOCK DIAGRAM



DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

REV. P2.10

DESCRIPTION

The XR68C92/192 is a Dual Universal Asynchronous Receiver and Transmitter with 8 (XR68C92) or 16 (XR68C192) bytes of transmit and receive FIFOs. The XR68C92/192 is pin-to-pin and functionally compatible to the XR68C681 and Philips SCC68681 UART with additional features. The operating speed of the receiver and transmitter can be selected independently from a table of twenty four fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock input. The XR68C92/192 provides a power down mode in which the oscillator is stopped but the register contents are retained. The XR68C92/192 is fabricated in an advanced CMOS process to achieve low power and high speed requirements.

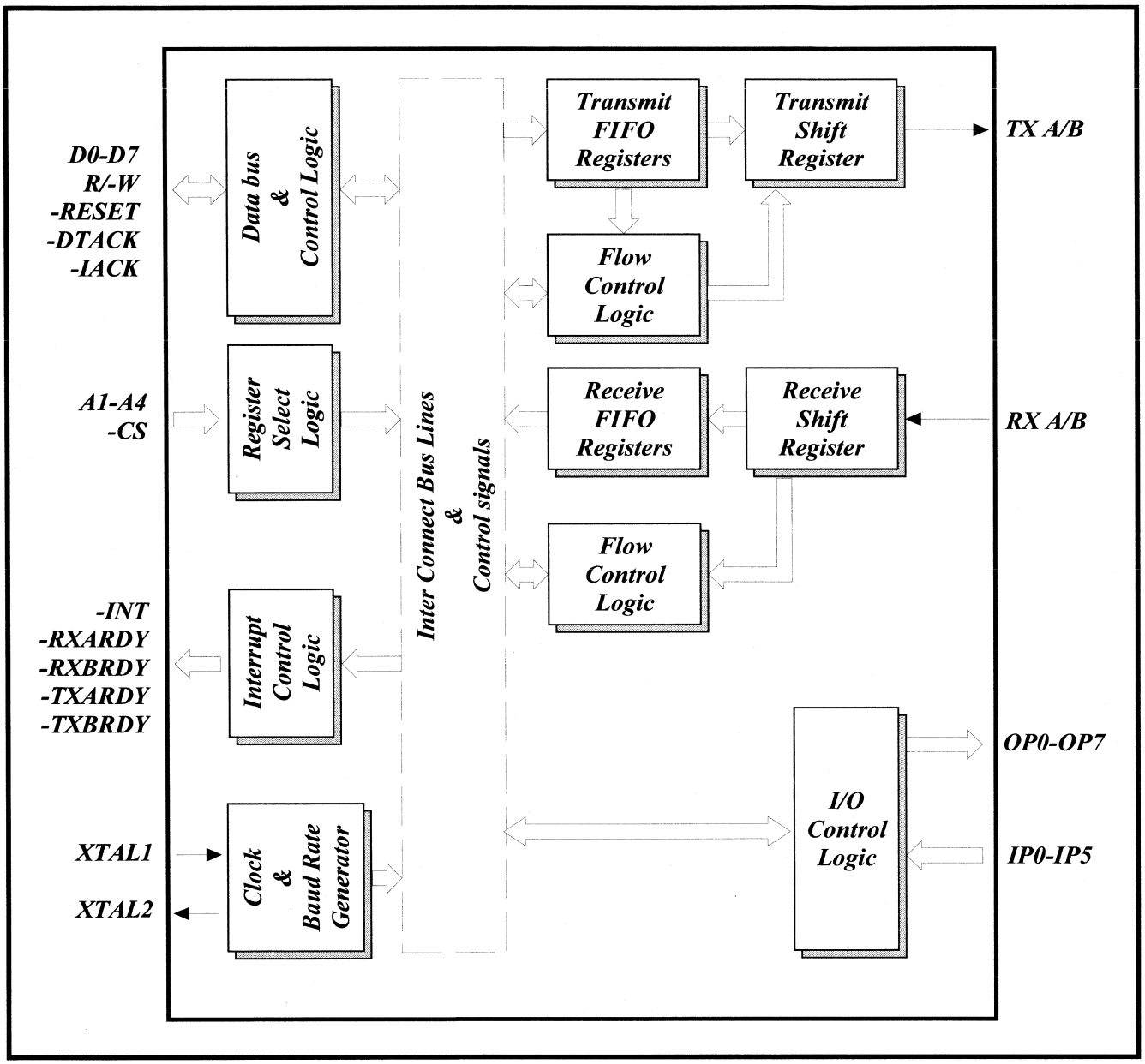
FEATURES

- Pin to pin and functionally compatible to XR68C681and SCC68692
- Full duplex transmit and receive operation
- 8 bytes of transmit/receive FIFOs (XR68C92)
- 16 bytes of transmit/receive FIFOs (XR68C192)
- Programmable character lengths (5, 6, 7, 8)
- Parity, framing, and over run error detection
- Programmable 16-bit timer/counter
- On-chip crystal oscillator
- Single interrupt output with eight selectable interrupting conditions
- External 1X or 16X clock
- Data rate up to 1Mbps
- Independent transmit and receive baud rates from 50bps to 230.4kbps
- 6 General purpose inputs
- 8 General purpose outputs
- TTL compatible inputs, outputs
- 4 Transmit/receive trigger levels
- Watch dog timer
- Multi-drop mode compatible with 8051 nine bit mode
- 3.3 or 5 volts operation
- Loopback modes
- Power down mode

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR68C92CP	40-Lead PDIP	0°C to + 70°C
XR68C92CJ	44-Lead PLCC	0°C to + 70°C
XR68C92CV	44-Lead TQFP	0°C to + 70°C
XR68C92IP	40-Lead PDIP	-40°C to + 85°C
XR68C92IJ	44-Lead PLCC	-40°C to + 85°C
XR68C92IV	44-Lead TQFP	-40°C to + 85°C
XR68C192CP	40-Lead PDIP	0°C to + 70°C
XR68C192CJ	44-Lead PLCC	0°C to + 70°C
XR68C192CV	44-Lead TQFP	0°C to + 70°C
XR68C192IP	40-Lead PDIP	-40°C to + 85°C
XR68C192IJ	44-Lead PLCC	-40°C to + 85°C
XR68C192IV	44-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

REV. 1.20

DESCRIPTION

The XR88C92/192 is a Dual Universal Asynchronous Receiver and Transmitter with 8 (XR88C92) / 16 (XR88C192) bytes transmit and receive FIFO. The XR88C92/192 is a pin and functional replacement for the SC26C92 and an improved version of the Philips SCC2692 UART with faste data access and other additional features. The operating speed of the receiver and transmitter can be selected independently from a table of eighteen fixed baud rates, a 16x clock derived from a programmable counter/timer, or an external 1x or 16x clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock input. The XR88C92/192 provides a power-down mode in which the oscillator is stopped but the register contents are retained. The XR88C92/192 is fabricated in an advanced CMOS process to achieve low power and high speed requirements.

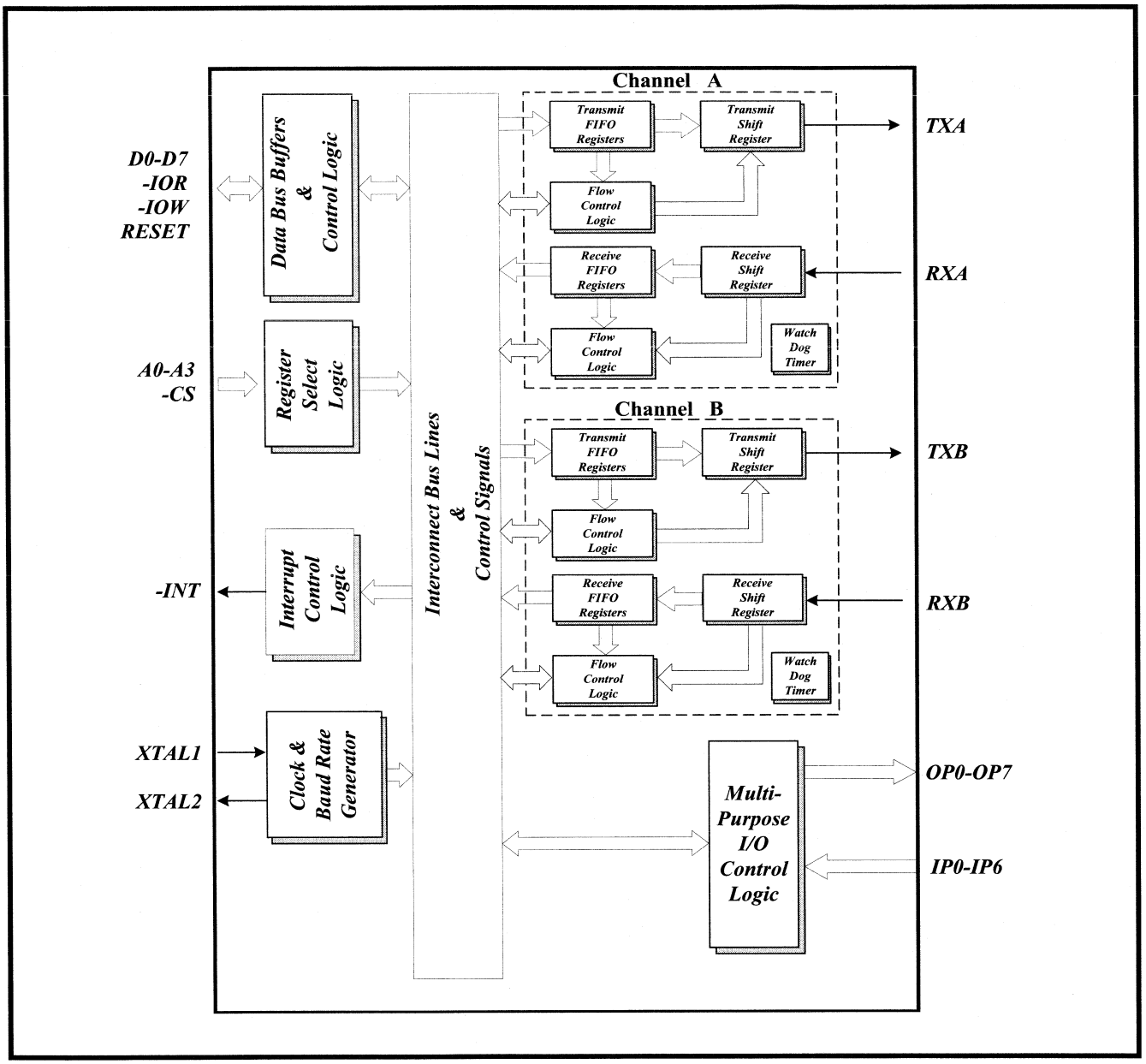
FEATURES

- Pin-to-pin and functionally compatible to SC26C92 and SCC2692
- Enhanced multidrop mode operation with separate storage for address and data tags (9th bit)
- 8 Bytes transmit/receive FIFO (XR88C92)
- 16 Bytes transmit/receive FIFO (XR88C192)
- Standard baud rates from 50bps to 230.4kbps
- Non-standard baud rate of up to 1Mbps
- Transmit and receive trigger levels
- Watch dog timer
- Programmable clock source for receiver and transmitter of each channel
- Single interrupt output
- Seven multi-purpose inputs
- Eight multi-purpose outputs
- 3.3V or 5V operation
- Various looback modes
- Programmable character lengths (5, 6, 7, 8)
- Parity, framing, and over-run error detection
- Programmable 16-bit timer/counter
- On-chip crystal oscillator
- TTL-compatible inputs, outputs
- Power-down mode

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR88C92CJ	44-Lead PLCC	0°C to + 70°C
XR88C92CP	40-Lead PDIP	0°C to + 70°C
XR88C92CV	44-Lead TQFP	0°C to + 70°C
XR88C92IJ	44-Lead PLCC	-40°C to + 85°C
XR88C92IP	40-Lead PDIP	-40°C to + 85°C
XR88C92IV	44-Lead TQFP	-40°C to + 85°C
XR88C192CJ	44-Lead PLCC	0°C to + 70°C
XR88C192CP	40-Lead PDIP	0°C to + 70°C
XR88C192CV	44-Lead TQFP	0°C to + 70°C
XR88C192IJ	44-Lead PLCC	-40°C to + 85°C
XR88C192IP	40-Lead PDIP	-40°C to + 85°C
XR88C192IV	44-Lead TQFP	-40°C to + 85°C

BLOCK DIAGRAM



QUAD UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

REV. 2.01

DESCRIPTION

The EXAR Quad Universal Asynchronous Receiver and Transmitter (QUART) is a data communications device that provides four fully independent full-duplex asynchronous communication channels in a single package. The QUART is designed for use in microprocessor based systems and may be used in a polled or interrupt-driven environment. The XR-82C684 device offers a single IC solution for various microprocessor families. The "88" and "68 modes" (for the 8800 and 68000 family of processors, respectively) can be selected by tying the SEL pin to V DD or V SS . The QUART is fabricated using advanced two layer metal, with a high performance density EPI/CMOS 1.8_ process to provide high performance and low power consumption, and is packaged in a 44-pin PLCC and a 68-pin PLCC.

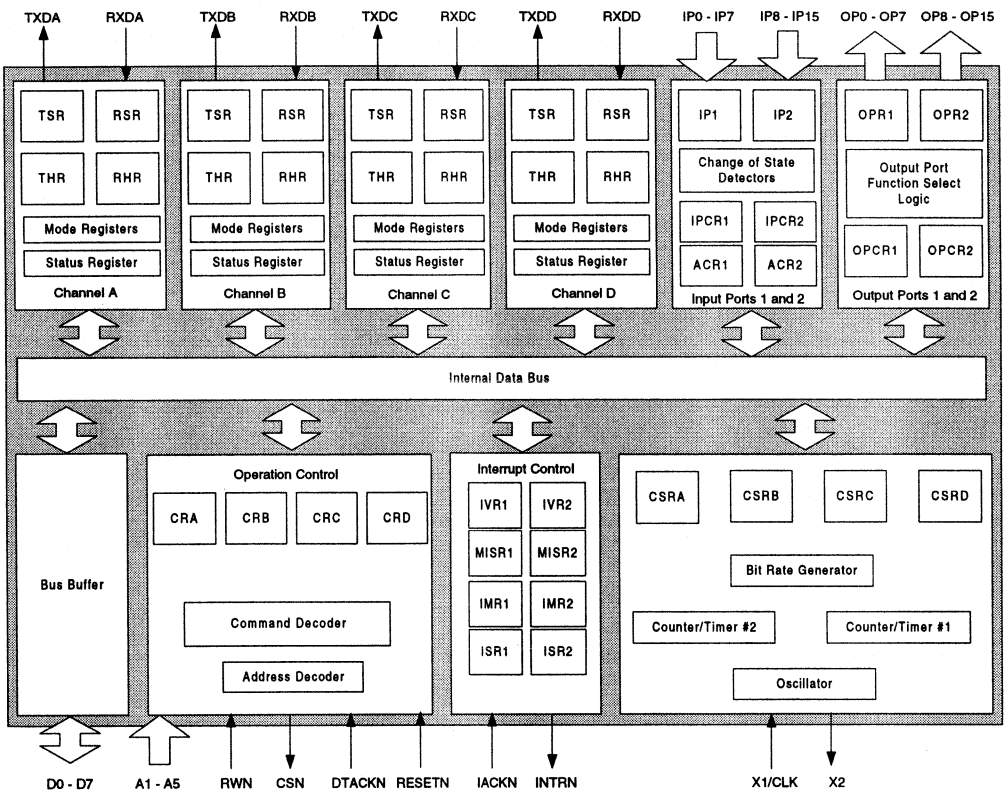
FEATURES

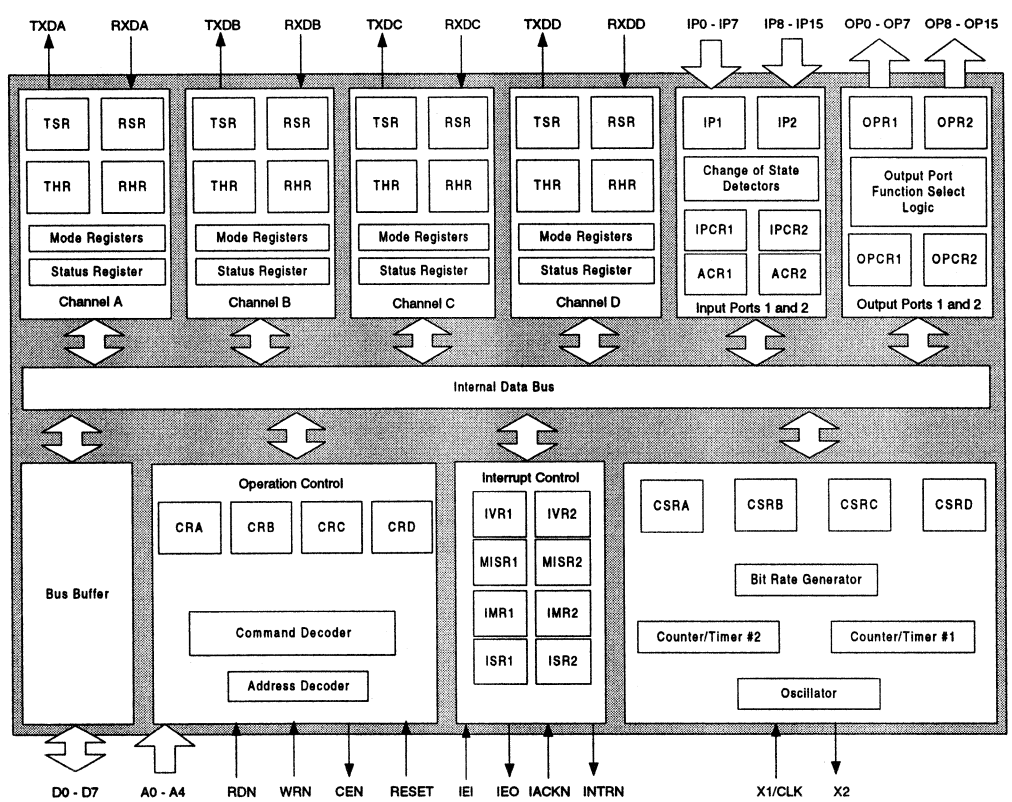
- Four Full-Duplex, Independent Channels
- Asynchronous Receiver and Transmitter
- Quadruple-Buffered Receivers and Transmitters
- Programmable Stop Bits in 1/16 bit increments
- Pin Selectable "88" and "68" Mode
- Internal Bit Rate Generators with more than 33 Bit Rates
- Independent Bit Rate Selection for each Transmitter and Receiver
- External Clock Capability
- Maximum Bit Rate: 1X clock - 1Mb/s, 16X clock - 125 kb/s
- Normal, AUTOECHO, Local LOOPBACK and Remote LOOPBACK Modes
- Two Multi-function 16-bit Counter/Timers
- Interrupt Output with Sixteen Maskable Interrupt Conditions
- Interrupt Vector Output on Acknowledge
- Programmable Interrupt Daisy Chain (Z-Mode Operation only)
- 16 General Purpose Output pins
- 16 General Purpose Input pins with Change of States Detectors on eight Inputs
- Multi-drop Mode Compatible with 8051 Nine Bit Mode
- On-chip Oscillator for Crystal
- Standby Mode to Reduce Operating Power
- Advanced CMOS Low Power Technology

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR82C684CJ/44	44-Lead PLCC	0°C to + 70°C
XR82C684CJ	68-Lead PLCC	0°C to + 70°C
XR82C684J/44	44-Lead PLCC	-40°C to + 85°C
XR82C684J	68-Lead PLCC	-40°C to + 85°C

BLOCK DIAGRAMS, 68 AND 88 MODES





UART WITH 128-BYTE FIFOs, FIFO COUNTERS AND HALF DUPLEX CONTROL

GENERAL DESCRIPTION

The XR16C850[1] (850) is a universal asynchronous receiver and transmitter (UART) and is pin compatible with the ST16C550,ST16C650A, and TI's TL16C750 UART. The 850 is an enhanced UART with 128 byte FIFOs, automatic hardware/software flow control, and data rates up to 1.5Mbps. It includes transmit/receive FIFO counters to increase data loading and unloading throughput. Onboard status registers provide error indications and operational status. Modem interface control is included and can be optionally configured to operate with the Infrared (IrDA) encoder/decoder. Internal loopback allows onboard diagnostics. The 850 is available in 40-pin PDIP, 44-pin PLCC, 48-pin TQFP and 52-pin QFP packages. The 44, 48 and 52 pin versions provide both the standard (STD) mode or PC mode. The STD mode is compatible with the ST16C450, ST16C550, ST16C650A and TL16C750 while the PC mode supports standard PC COM port connections. The 40 PDIP pin package does not offer the PC mode.

1. Covered by U.S. patents #5,643,122, #5,949,787
2. Windows is a trademark of Microsoft Corporation.

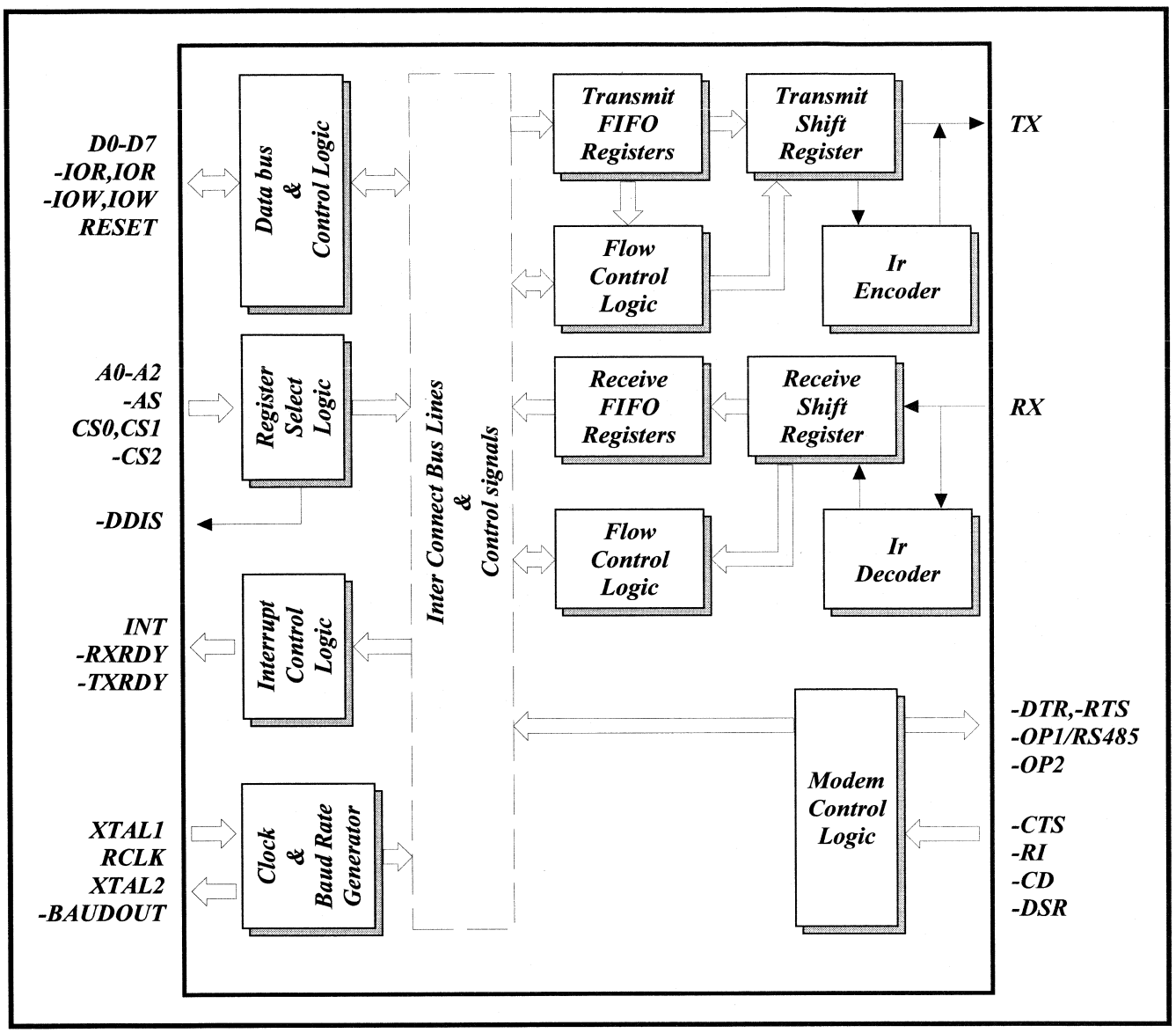
FEATURES

- Pin to pin compatible to ST16C550, ST16C650A and TL16C750
- Transmit/receive FIFO counters
- 128 bytes of Transmit/Receive FIFO
- RS-485 half duplex direction control
- Automatic software/hardware flow control
- Programmable transmit/receive trigger levels
- Infrared transmitter and receiver encoder/decoder
- Up to 1.5Mbps data rate
- Sleep mode (100µA standby)
- Small 7x7mm TQFP
- +5 or 3.3 Volts operation
- Windows[2] drivers available

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR16C850CP	40-Lead PDIP	0°C to + 70°C
XR16C850CJ	44-Lead PLCC	0°C to + 70°C
XR16C850CM	48-Lead TQFP	0°C to + 70°C
XR16C850CQ	52-Lead QFP	0°C to + 70°C
XR16C850IP	40-Lead PDIP	-40°C to + 85°C
XR16C850IJ	44-Lead PLCC	-40°C to + 85°C
XR16C850IM	48-Lead TQFP	-40°C to + 85°C
XR16C850IQ	52-Lead QFP	-40°C to + 85°C

BLOCK DIAGRAM



QUAD UART WITH RX/TX FIFO COUNTERS, 128-BYTE FIFO

DESCRIPTION

The XR16C854[1] (854) is a universal asynchronous receiver and transmitter (UART) with a dual foot print interface compatible with the ST16C554/554D, ST16C654/654D and ST68C554. The 854 is an enhanced UART with 128 byte FIFO's, Independent Transmit and Receive FIFO counters, automatic hardware/software flow control, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status, modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. The 854 is available in 64 pin TQFP, 68 pin PLCC, and 100 pin QFP packages. The 64 pin package offers the 16 interface mode which is compatible with the industry standard ST16C554. The 68 and 100 pin packages offer an additional 68 mode which allows easy integration with Motorola, and other popular microprocessors. The XR16C854CV (64 pin) offers three state interrupt control while the XR16C854DCV provides constant active interrupt outputs. The 64 pin devices do not offer TXRDY/RXRDY outputs or the default clock select option (CLKSEL). The 100 pin packages offer faster channel status access by providing separate outputs for TXRDY and RXRDY, offer separate Infrared TX outputs and an independent channel C clock input. The 854 combines the package interface modes of the 16C554/654 and 68C554 series on a single integrated chip.

1. Covered by U.S. patents #5,643,122, #5,949,787

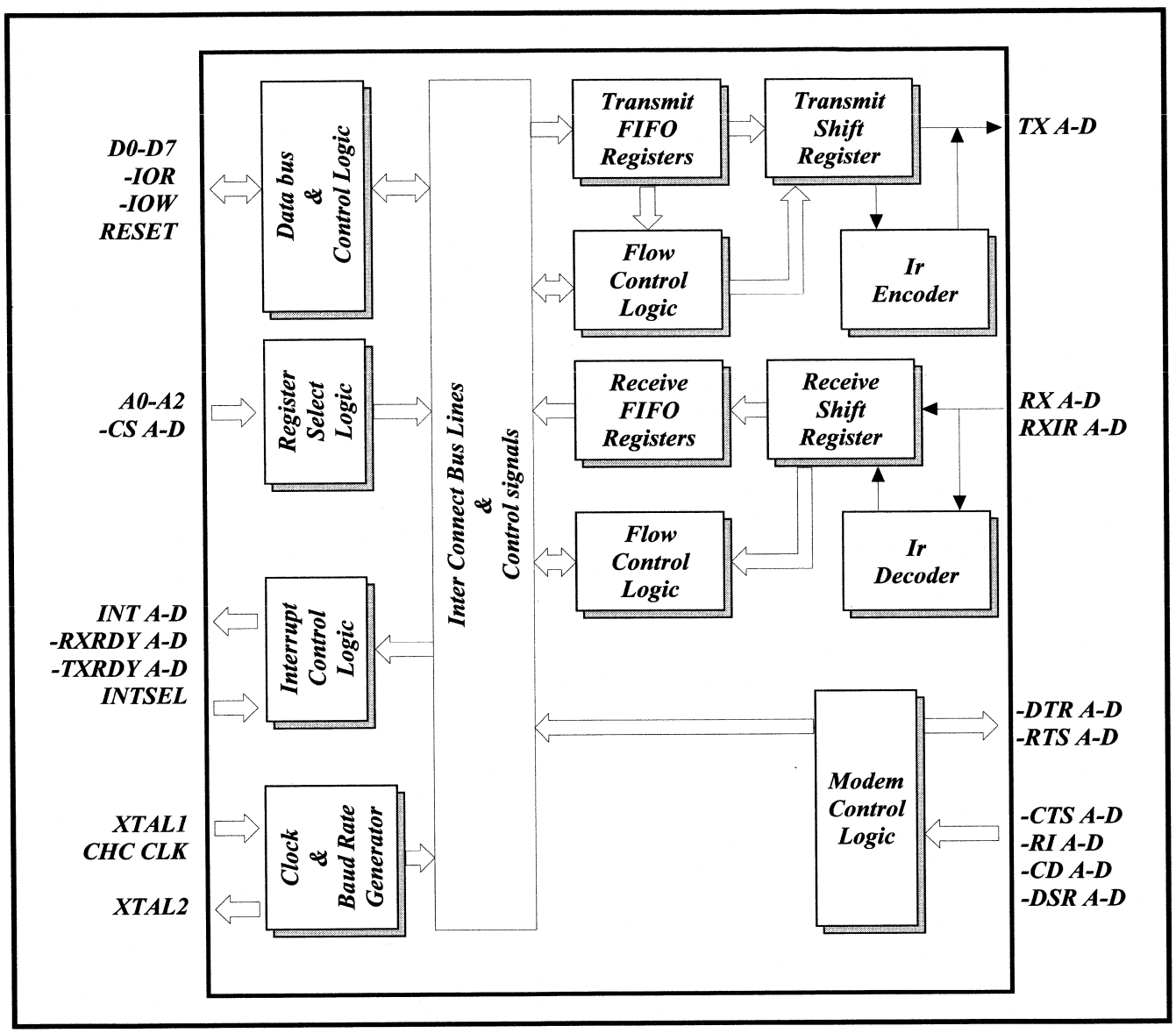
FEATURES

- Compatibility with the Industry Standard ST16C554/554D, ST68C654/654D, TL16C554/754
- 1.5 Mbps transmit/receive operation (24MHz)
- 128 byte transmit and receive FIFO
- Independent transmit and receive FIFO counters
- Automatic software/hardware flow control
- Programmable Xon/Xoff characters
- Programmable Baud Rate Generator with pre-scaleable clock rates of 1X or 4X.
- Programmable Transmit/Receive FIFO interrupt trigger levels
- Standard modem interface or infrared IrDA encoder/decoder interface
- Software flow control turned off optionally by any (Xon) RX character
- Independent channel C clock on 100 pin packages
- +3.3V or +5V supply operation
- 100 pin packages offer internal register FIFO monitoring and separate IrDA TX outputs
- Sleep mode (200µA stand-by)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR16C854CJ	68-Lead PLCC	0°C to + 70°C
XR16C854CV	64-Lead TQFP	0°C to + 70°C
XR16C854DCV	64-Lead TQFP	0°C to + 70°C
XR16C854CQ	100-Lead QFP	0°C to + 70°C
XR16C854IJ	68-Lead PLCC	-40°C to + 85°C
XR16C854IV	64-Lead TQFP	-40°C to + 85°C
XR16C854DIV	64-Lead TQFP	-40°C to + 85°C
XR16C854IQ	100-Lead QFP	-40°C to + 85°C

BLOCK DIAGRAM



QUAD UART WITH RX/TX FIFO COUNTERS,128-BYTE FIFO

DESCRIPTION

The XR16C864[1] (864) is a universal asynchronous receiver and transmitter (UART) with a dual interface compatible with the ST16C554/654/854 and ST68C554. The 864 is an enhanced UART with 128 byte FIFO's, Independent Transmit and Receive FIFO counters, RS-485 Support, Independent Transmit and Receive DMA signals, automatic hardware/software flow control, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status, modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. The 864 is available in 100 pin QFP packages. The XR16C864 offers faster channel status access by providing separate outputs for TXRDY and RXRDY, offer separate Infrared TX outputs and a separate clock for channel C (CHC-CLK) that can be used as a musical instrument clock input. The 864 combines the package interface modes of the 16C554/654 and 68C554 series on a single integrated chip.

1. Covered by U.S. patents #5,643,122, #5,949,787

FEATURES

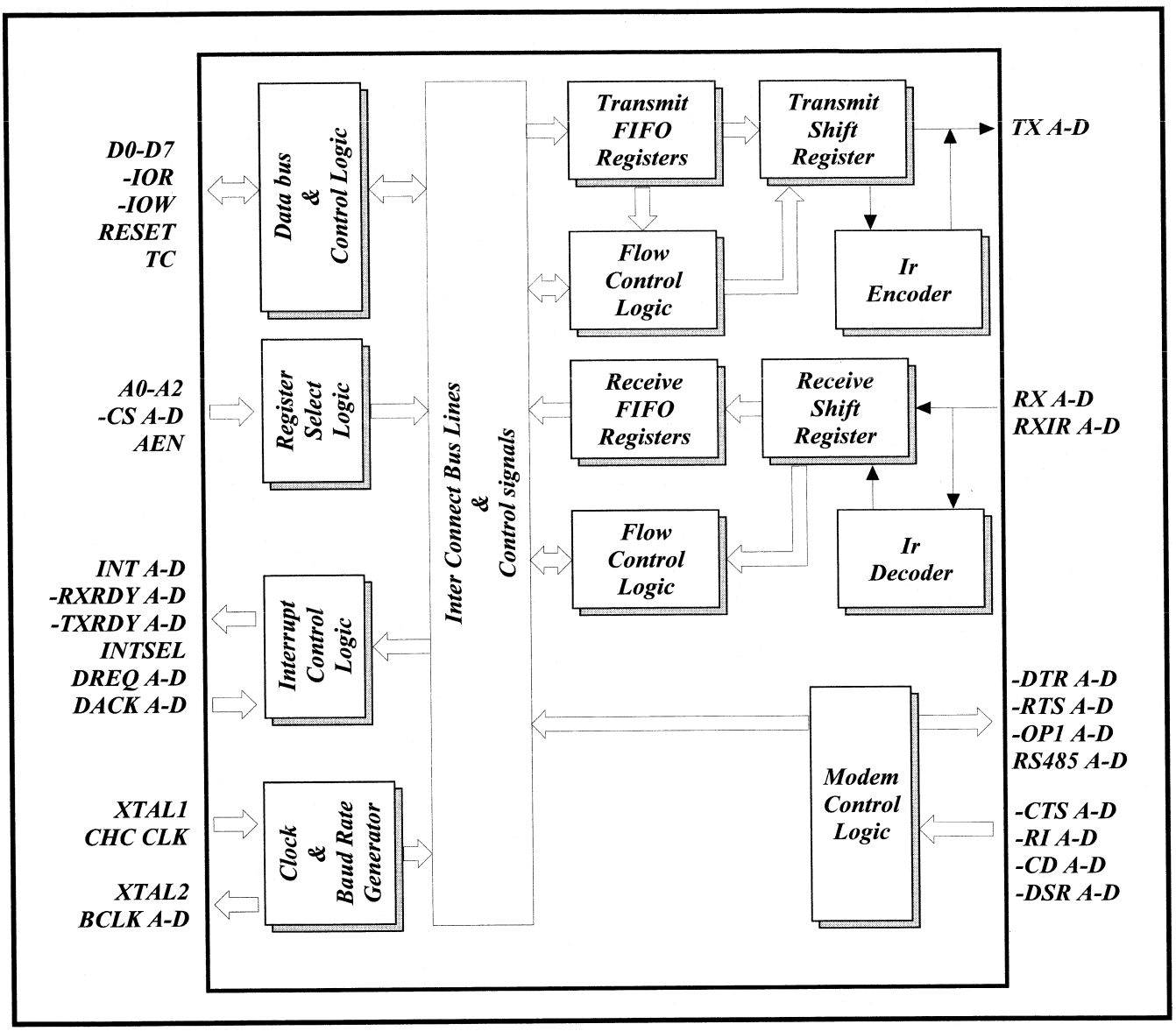
- Compatibility with the Industry Standard ST16C554/654, ST68C554, TL16C554
- 1.5 Mbps transmit/receive operation (24MHz)
- 128 byte transmit FIFO
- 128 byte receive FIFO with error flags
- Automatic RS-485 half-duplex switch
- Independent transmit and receive DMA signals
- Independent transmit and receive FIFO counter
- Automatic software/hardware flow control
- Programmable Xon/Xoff characters
- Software selectable Baud Rate Generator pre-scaleable clock rates of 1X, 4X.
- Four selectable, and Programmable Transmit/Receive FIFO interrupt trigger levels
- Standard modem interface or infrared IrDA encoder/decoder interface
- Software flow control turned off optionally by any (Xon) RX character
- Independent clock input for channel C
- FIFO monitoring and separate IrDA TX outputs
- Sleep mode (200µA stand-by)
- 100-pin QFP packages

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR16C864CQ	100-Lead QFP	0°C to + 70°C
XR16C864IQ	100-Lead QFP	-40°C to + 85°C

NOTE: **Covered by patents #5,649,122, #5,949,787*

BLOCK DIAGRAM 16 MODE



DUAL UART WITH 1284 PARALLEL PORT AND PLUG-AND-PLAY CONTROLLER

REV. P1.00

DESCRIPTION

The XR16C872[1] is a dual universal asynchronous receiver and transmitter with a 1284 bi-directional parallel port and ISA Bus Plug-and-Play (PnP) interface. The PnP interface supports auto configuration for desktop and embedded PC computers. The host bus interface can also be configured to manually support standard PC addresses COM1-4 and LPT1-2. The parallel port is compatible to IEEE 1284 specification and supports Compatible Centronics, Extended Capability (ECP) and Enhanced Parallel Port (EPP) protocols. The UARTs are software compatible to industry standard 16C550 and include enhanced features of 128 bytes of transmit and receive FIFOs, programmable transmit and receive FIFO trigger levels, transmit and receive FIFO counters, IrDA (Infrared Data Association) encoder/decoder, automatic RTS/CTS hardware flow control with selectable hysteresis, automatic software (Xon/Xoff) flow control and infrared encoder/decoder. On board status registers provide interrupt priorities, receive data errors and modem status. Each channel has a programmable baud rate generator to provide data rates up to 460.8Kbps. The bi-directional parallel port can be configured as a general purpose input/output interface or connected to a printer or portable storage devices. The XR16C872 operates on a single +5V and +3.3 power supply. It is available in a small 100-pin QFP package and offers commercial and industrial temperature ranges. The chip is fabricated in an advanced CMOS process to reduce power consumption.

1. Covered by U.S. patents #5,643,122, #5,949,787
2. Windows is a trademark of Microsoft Corporation

FEATURES

- Plug and play ISA bus specification compliant
- Auto configuration
- Direct connection, needing no external buffers
- Resource data in external 4K EEPROM
- 10-interrupts IRQ3-7, IRQ9-12, IRQ15
- Manual configuration for standard COM1-COM-4 and LPT1-LPT2
- IEEE 1284 compliant
- Bi-directional host port
- Level II electrical interface, needing no external transceivers
- Standard centronics/ECP/EPP mode
- 16-byte FIFO in ECP mode
- Dual UART software compatible with 16C550
- 128-Byte transmit and receiver FIFOs reduce CPU interrupt
- FIFO counters in transmitter and receiver
- Automatic RTS/CTS flow control with hysteresis to increase data throughput
- IrDA infrared pulse shaping encoder/decoder for up to 115.2Kbps data rate
- Up to 460.8 Kbps standard serial data rate
- +5V and +3.3V operation
- 100-pin quad flat package (14x20mm)
- Reference PC ISA card design available
- Windows[2] 98 and NT4.0 device drivers available

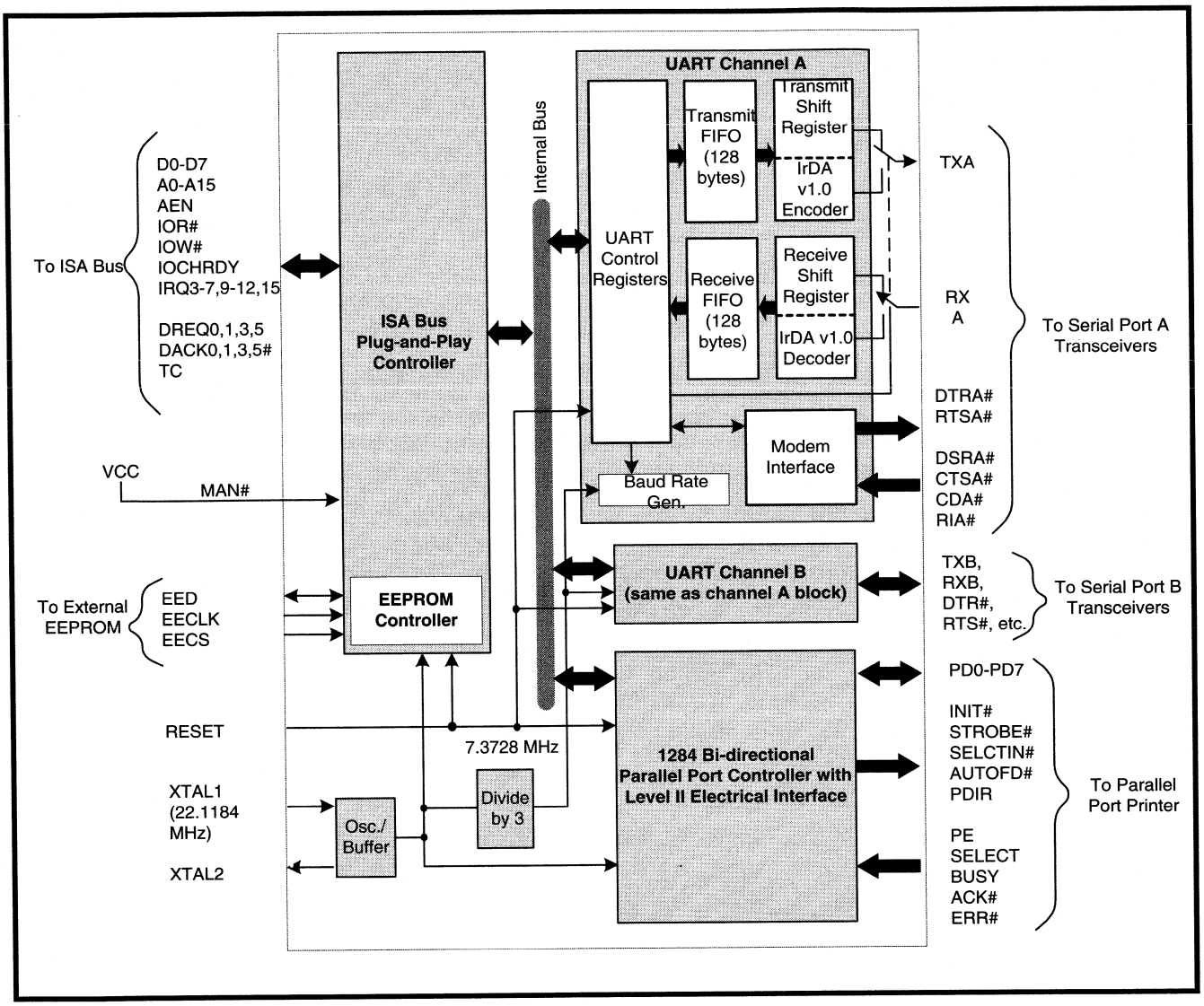
APPLICATIONS

- Multi-function PC/ISA bus card with RS-232/RS-422/RS-485 interface and printer/parallel port
- Embedded systems
- Portable infrared wireless systems
- High-speed bi-directional Parallel port
- High-speed serial ports

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
XR16C872CQ	100-Lead QFP	0°C to + 70°C
XR16C872IQ	100-Lead QFP	-40°C to + 85°C

FUNTIONAL BLOCK DIAGRAM WITH PLUG-AND-PLAY INTERFACE



2.5V, 3.3V AND 5V LOW POWER UART WITH 32-BYTE FIFO

GENERAL DESCRIPTION

The XR16L651[1] (651) is a 2.5V, 3.3V and 5V Universal Asynchronous Receiver and Transmitter (UART) with 5V tolerant inputs. This new device supports Intel and Motorola data bus interface and is software compatible to industry standard 16C450, 16C550, ST16C580 and ST16C650A UARTs.

The 651 has 32 bytes of TX and RX FIFOs and is capable of operating up to serial data rate of 2 Mbps at 3.3V supply voltage. The internal registers include the 16C550 register set plus Exar's enhanced registers for additional features to support today's highly demanding data communication needs. The enhanced features include automatic hardware and software flow control, selectable TX and RX trigger levels, and wireless infrared (IrDA) encoder/decoder.

The device provides a new capability to give user the ability to program the wireless infrared encoder output pulse width, hence, reduces the power consumption of the handheld unit.

The XR16L651 device comes in a small 7x7x1mm 48-pin TQFP package with commercial and industrial temperature ranges.

NOTE: *1) Covered by US patents #5,649,122 and #5,949,787*

NOTE: *2) Underline features are exclusive to XR16L651.*

FEATURES

- 2.5V, 3.3V and 5V Operation w/ 5V tolerant Inputs[2]
- ST16C450/550/580/650A Software Compatible
- Intel, Motorola[2] or PC Mode 8-bit Bus Interface
- Up to 1Mbps Data Rate at 3.3V Operation
- 32-byte Transmit and Receive FIFOs
- Automatic Hardware (RTS/CTS) Flow Control
- Hardware Flow Control Hysteresis
- Automatic Software (Xon/Xoff) Flow Control
- Infrared (IrDA) Encoder/Decoder Enable Input[2]
- Programmable Infrared Encoder Pulse With
- Sleep Mode with Wake-up Indicator
- 48-pin TQFP Package (7x7x1mm)
- Commercial and Industrial Temperature Grades

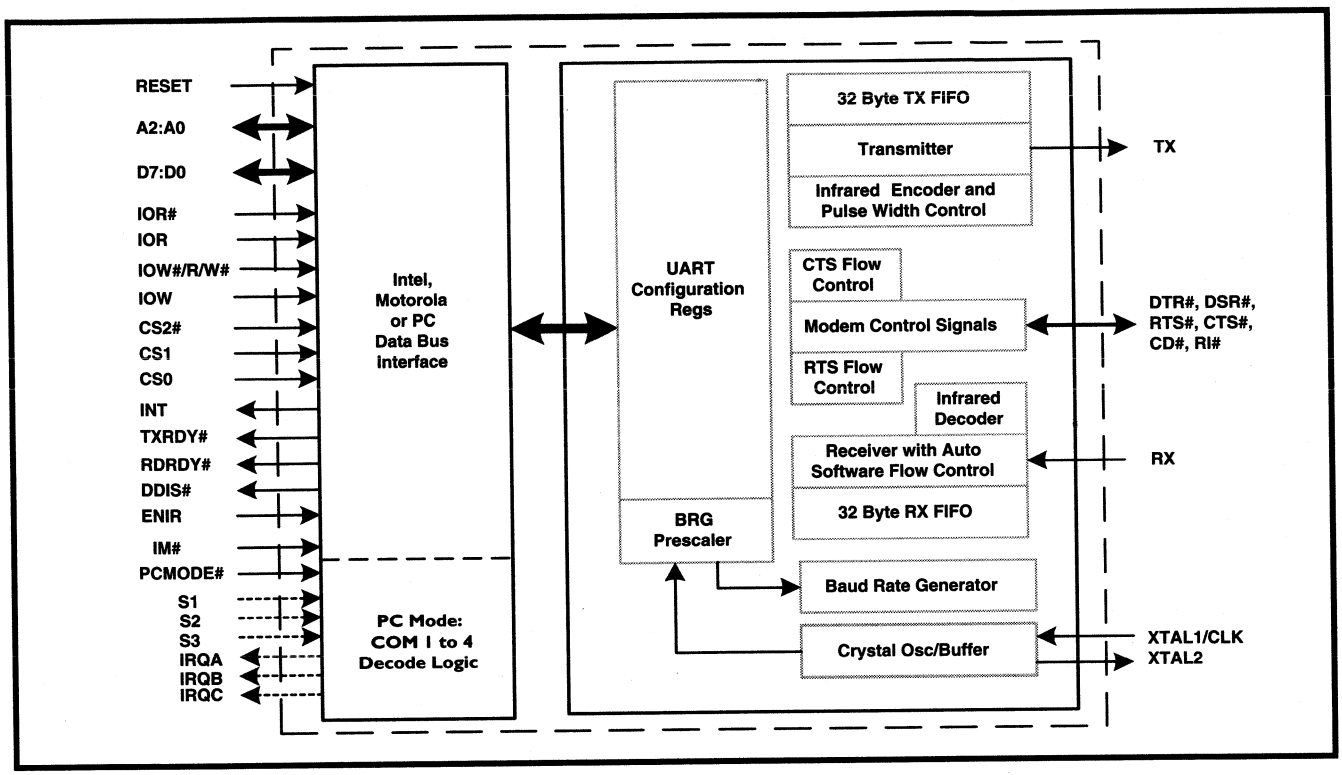
APPLICATIONS

- Battery Operated Electronics
- Internet Appliances
- Handheld Terminal
- Personal Digital Assistants
- Cellular Phones DataPort
- Wireless Infrared Data Communications Systems

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGR
XR16L651CM	48-Lead TQFP	0°C to +70°C
XR16L651IM	48-Lead TQFP	-40°C to +85°C

BLOCK DIAGRAM



QUAD HIGH-PERFORMANCE 3.3V AND 5.0V UART

GENERAL DESCRIPTION

The XR16L784[1] (784) is a quad Universal Asynchronous Receiver and Transmitter (UART). The device is designed for high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 4 channels to speed up interrupt parsing. Each UART has its own 16C550 compatible set of configuration registers, transmit and receive FIFOs of 64 bytes, fully programmable transmit and receive FIFO level triggers, transmit and receive FIFO level counters, automatic RTS/CTS or DTR/DSR hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, IrDA (Infrared Data Association) encoder/decoder, and a 16-bit general purpose timer/counter.

NOTE: *1 Covered by U.S. Patent #5,649,122 and #5,832,205*

APPLICATIONS

- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

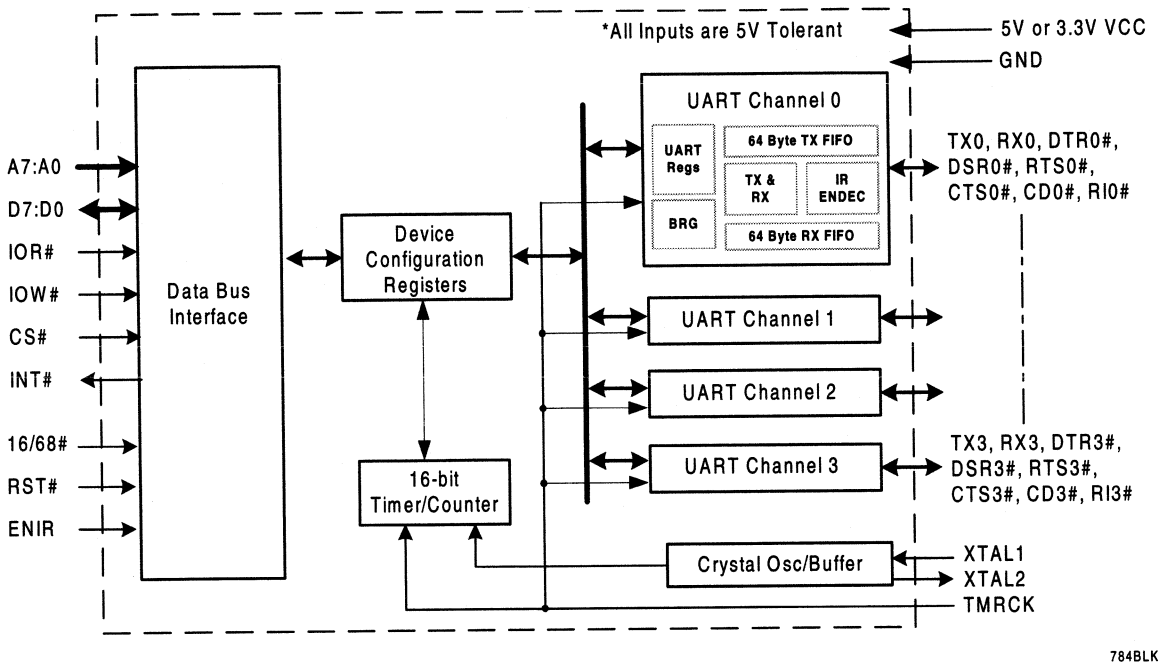
FEATURES

- High Performance Quad UART
- 5V and 3.3V Operation with 5V Tolerant Inputs
- 8-bit Intel or Motorola Data Bus Interface
- Single Open Drain Interrupt for all 4 channels
- Global Interrupt Source Registers for all channels
- Fifth Generation "Flat" Register Set
- Each UART is Independently Controlled and Includes
- 16C550 Compatible Registers
- 64-byte Transmit and Receive FIFOs
- Transmit and Receive FIFO Level Counters
- Programmable TX and RX FIFO Level Trigger
- Automatic RTS/CTS or DTR/DSR Flow Control
- Selectable Hardware Flow Control Hysteresis
- Automatic Xon/Xoff Software Flow Control
- RS485 Half-duplex Control with Selectable Delay
- Infrared (IrDA 1.1) Data Encoder/Decoder
- Programmable Data Rate with Prescaler
- Up to 3.12 (16x) and 6.25 (8x) Mbps Data Rate
- A General Purpose 16-bit Timer/Counter
- Sleep Mode with Automatic Wake-up
- 64-pin TQFP Package (10x10x1.4 mm)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGR
XR16L784CV	64-Lead TQFP (10 x 10 x 1.4mm)	0°C to +70°C
XR16L784IV	64-Lead TQFP (10 x 10 x 1.4mm)	-40°C to +85°C

XR16L784 BLOCK DIAGRAM



XR16L788

(Formerly XR16L758)

OCTAL HIGH PERFORMANCE 3.3V AND 5.0V UART

REV. 1.1.3

GENERAL DESCRIPTION

The XR16L788[1] (788), formerly XR16L758, is a 5V and 3.3V with 5V tolerant inputs octal Universal Asynchronous Receiver and Transmitter (UART). The highly integrated device is designed for high bandwidth requirement in communication systems. A new feature increases device driver efficiency includes a global interrupt pin with global interrupt source registers that provide complete and detailed interrupt status information for all 8 channels that will speed up interrupt parsing. Other new facilities include simultaneous UART registers initialization, individual UART channel soft-reset, DTR/DSR hardware flow control, software flow control (Xoff/Xon) detection indicators, RS-485 half-duplex direction control with programmable turn-around delay, Intel or Motorola bus interface and sleep mode now has a wake-up indicator.

NOTE: Covered by US patents #5,649,122 and #5,949,787

APPLICATIONS

- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

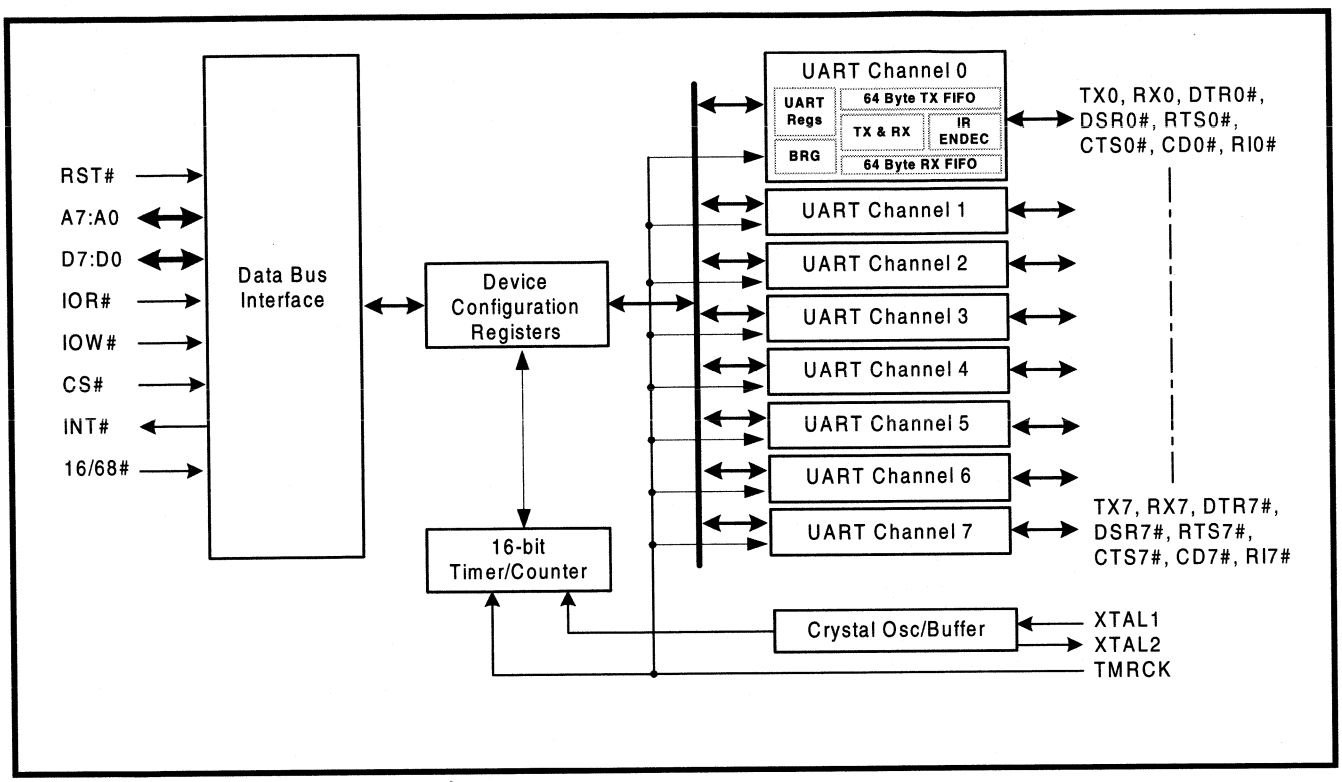
NEW FEATURES:

- 5V and 3.3V with 5V Tolerant Inputs Operation
- Single Interrupt Output for all 8 UARTs
- Global Interrupt Source for all 8 UARTs
- 5G "Flat" UART Registers for Configurations
- Simultaneous UART Channels Initialization
- Auto RS485 Half-duplex Control with Programmable Turn-around Delay
- A General Purpose 16-bit Timer/Counter
- Sleep Mode with Wake-up Indication
- Highly Integrated Device for Space Saving
- First eight registers are 16C550 compatible
- 64-byte Transmit and Receive FIFOs
- Transmit and Receive FIFO Level Counters
- Programmable TX and RX FIFO Trigger Levels
- Automatic RTS/CTS or DTR/DSR Flow Control
- Selectable Hardware Flow Control Hysteresis
- Automatic Xon/Xoff Software Flow Control with Status Indicator
- Infrared (IrDA 1.0) Data Encoder/Decoder
- Programmable Data Rate with Prescaler
- Up to 6.25 Mbps Serial Data Rate at 5V
- 100-pin QFP Package (14x20x3 mm)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XR16L788CQ	100-Lead QFP (14 x 20 x 3mm)	0°C to +70°C
XR16L788IQ	100-Lead QFP (14 x 20 x 3mm)	-40°C to +85°C

BLOCK DIAGRAM



GENERAL DESCRIPTION

The XR17C154[1] (154) is a quad PCI Bus Universal Asynchronous Receiver and Transmitter (UART) with same package and pin-out as the Exar XR17C158 octal UART. The device is designed to meet today's 32-bit PCI Bus and high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 4 channels to speed up interrupt parsing. Each UART is independently controlled and has its own 16C550 compatible 5G register set, transmit and receive FIFOs of 64 bytes, fully programmable transmit and receive FIFO trigger levels, transmit and receive FIFO level counters, automatic hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, IrDA (Infrared Data Association) encoder/decoder, 8 multi-purpose definable inputs/outputs, and a 16-bit general purpose timer/counter.

NOTE: *1 Covered by U.S. Patents #5,649,122, #5,832,205*

APPLICATIONS

- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

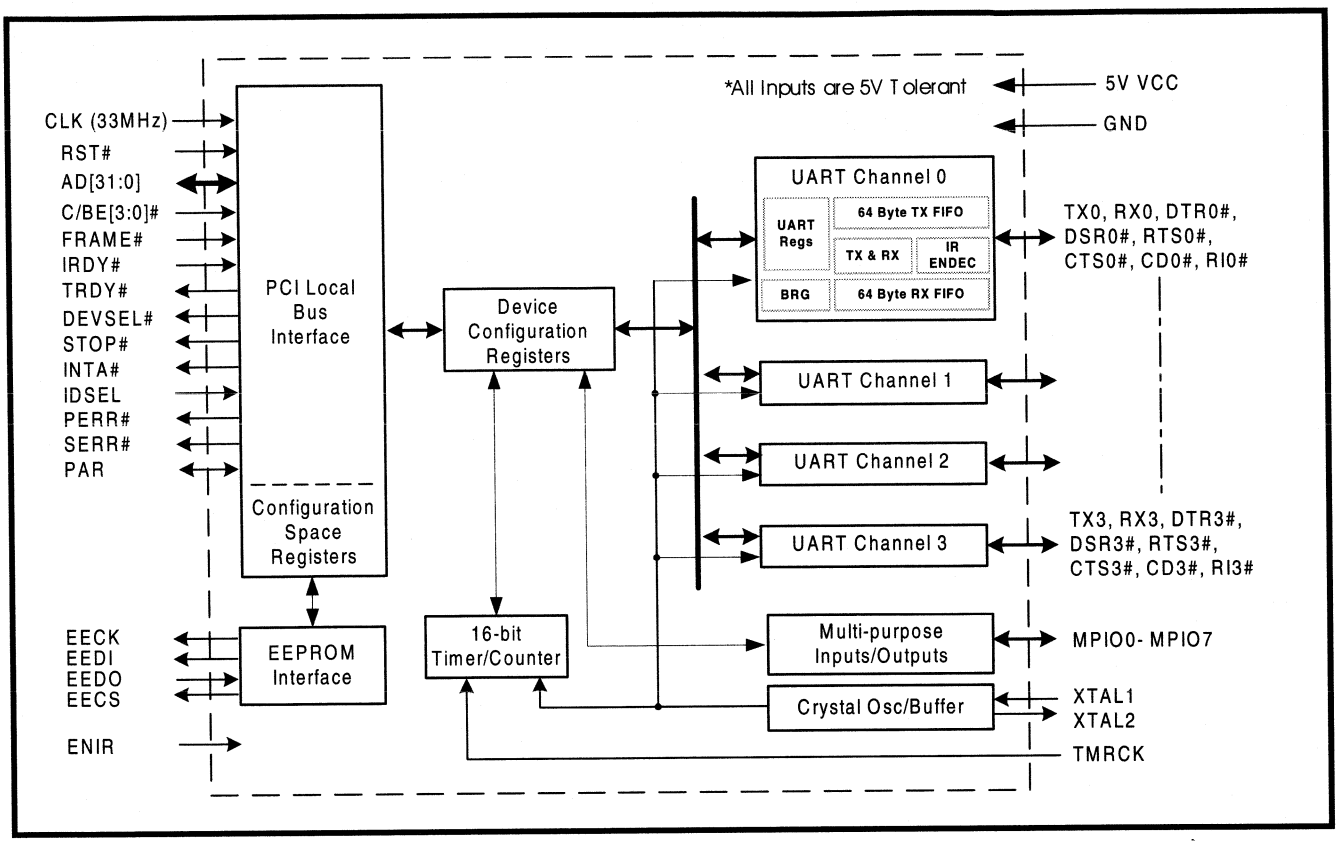
FEATURES

- High Performance Quad UART
- PCI Bus 2.2 Target Interface Compliance
- 5V PCI Bus Compliant up to 33MHz Clock
- 32-bit PCI Bus Interface with EEPROM Interface
- An Interrupt Status Register for all 4 UARTs
- Data Transfer in Byte, Word and Double-word
- Read/Write Burst Operation
- Each UART is independently Controlled and Includes:
- 16C550 Compatible Fifth Gen. (5G) Register Set
- 64-byte Transmit and Receive FIFOs
- Transmit and Receive FIFO Level Counters
- Automatic RTS/CTS or DTR/DSR Flow Control
- Automatic Xon/Xoff Software Flow Control
- RS485 Half-duplex Control with Selectable Delay
- Infrared (IrDA 1.0) Data Encoder/Decoder
- Programmable Data Rate with Prescaler
- Up to 3.125 Mbps Serial Data Rate at 5V
- Eight Multi-Purpose Inputs/outputs
- A General Purpose 16-bit Timer/Counter
- Sleep Mode with Automatic Wake-up
- 3.3V with 5V Tolerant Inputs Operation to 22MHz
- Same Package and Pin-out with XR17C158 UART

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XR17C154CV	144-Lead TQFP	0°C to +70°C
XR17C154IV	144-Lead TQFP	-40°C to +85°C

BLOCK DIAGRAM



GENERAL DESCRIPTION

The XR17C158[1] (158) is an octal Universal Asynchronous Receiver and Transmitter (UART). The device is designed to meet the 32-bit PCI Bus and high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 8 channels to speed up interrupt parsing. Each UART has its own 16C550 compatible set of configuration registers, transmit and receive FIFOs of 64 bytes, fully programmable transmit and receive FIFO level triggers, transmit and receive FIFO level counters, automatic RTS/CTS or DTR/DSR hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, IrDA (Infrared Data Association) encoder/decoder, 8 multi-purpose definable inputs/outputs, and a 16-bit general purpose timer/counter.

NOTE: *1 Covered by U.S. Patent #5,649,122 and #5,949,787*

APPLICATIONS

- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

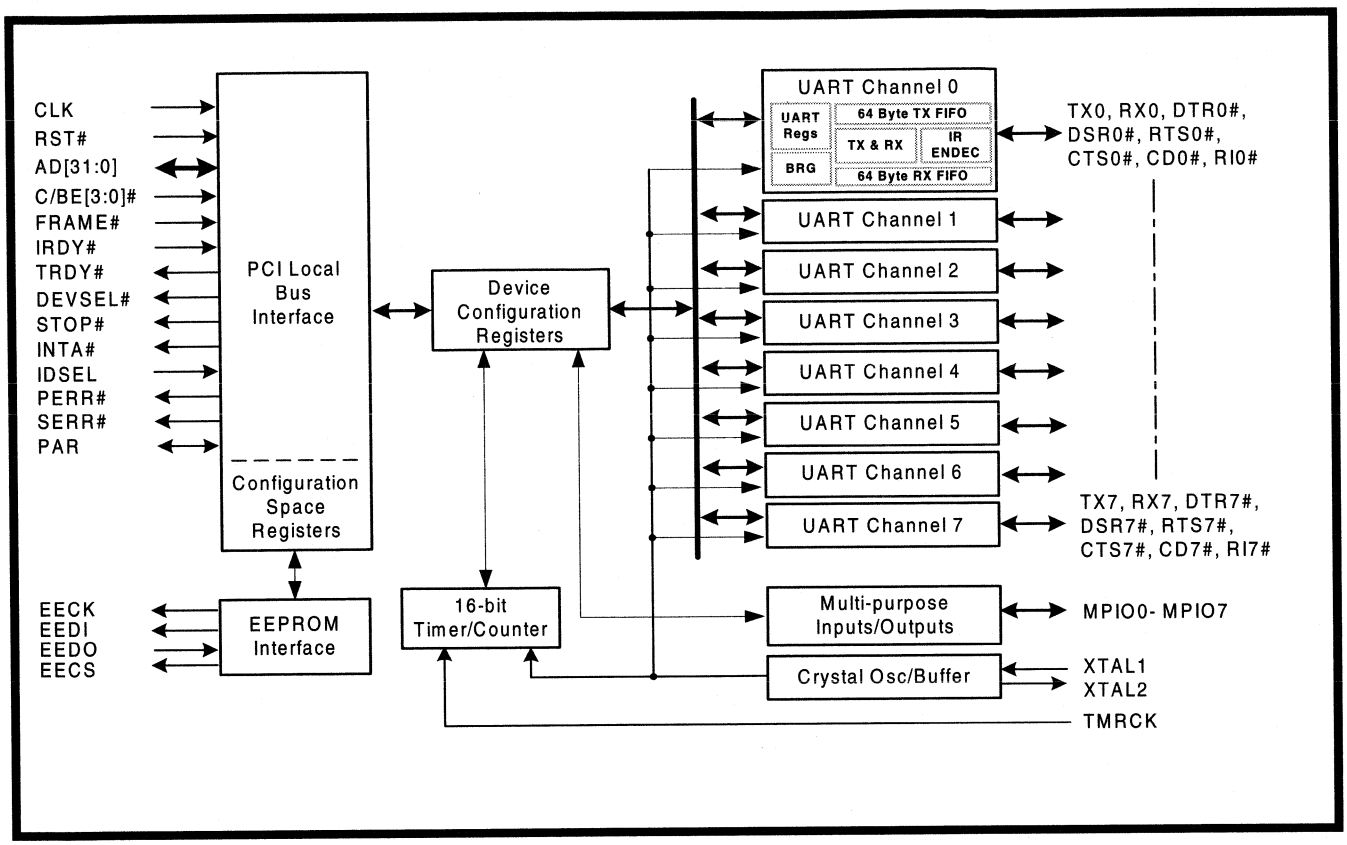
FEATURES

- High Performance Octal UART
- 32-bit PCI Bus Interface with EEPROM Interface
- - Interrupt Source Register for all 8 UARTs
- - Data Transfer in Byte, Word and Double-word
- - Read/Write Burst Operation
- Each UART Includes
- - 16C550 Compatible Registers
- - 64-byte Transmit and Receive FIFOs
- - Transmit and Receive FIFO Level Counters
- - Automatic RTS/CTS or DTR/DSR Flow Control
- - Automatic Xon/Xoff Software Flow Control
- - RS485 Half-duplex Control with Selectable Delay
- - Infrared (IrDA 1.0) Data Encoder/Decoder
- - Programmable Data Rate with Prescaler
- - Up to 6.25 Mbps Serial Data Rate
- Eight Multi-Purpose Inputs/outputs
- A General Purpose 16-bit Timer/Counter
- Sleep Mode with Automatic Wake-up
- 5V Operation (PCI Compliance)
- 3.3V Operation with 5V Tolerant Inputs
- 144-pin TQFP Package (20x20x1.4mm)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XR17C158CV	144-Lead TQFP	0°C to +70°C
XR17C158IV	144-Lead TQFP	-40°C to +85°C

BLOCK DIAGRAM



EXAR

GENERAL INFORMATION

COMMUNICATIONS PRODUCTS

WORLDWIDE SALES OFFICES

EXAR markets products worldwide with sales offices and personnel located throughout North America, Europe, Asia and Japan. In addition to these sales offices, EXAR also employs a worldwide team of field application engineers.

EXAR markets its products in the United States through a number of manufacturer's representatives and distributors. Internationally, the company sells products through various regional and country specific distributors with locations in 33 countries around the globe.

For product and technical inquiries, please call **1-800-366-9742** to be connected to your local sales representative office. Or using the world wide web, go to Exar's website at **http://www.exar.com**, click on the "Info Request" button on the homepage, and select the form you wish to submit.